R13

Code No: 126EN

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, December - 2017

VLSI DESIGN

(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART – A **(25 Marks)**

1.a)	What is pull up and pull down device?	[2]
b)	Why NMOS technology is preferred more than PMOS technology?	[3]
c)	What are the uses of Stick diagram?	[2]
d)	What is the fundamental goal in Device modeling?	[3]
e)	List out the sources of static and dynamic power consumption.	[2]
f)	Define Fan-in and Fan-out.	[3]
g)	Why is barrel shifter very useful in the designing of arithmetic circuits?	[2]
h)	Write the principle of any one fast multiplier.	[3]
i)	What is programmable logic array?	
j)	What are feed-through cells? State their uses.	

PART – B **(50 Marks)**

2.a)	What is meant by latch up problem? How will you prevent.	[5+5]
b)	Define threshold voltage? Drive the Vt equation for MOS transistor.	
	OR	
3.a)	Explain with neat diagrams the various NMOS fabrication technology.	[5+5]
b)	Draw and explain BiCMOS inverter circuit.	
4.	Draw the circuit diagram, stick diagram and layout for CMOS inverter.	[10]
	OR	
5.a)	Explain about the various layout design rules.	
b)	Draw the static CMOS logic circuit for the following expression i) $Y=(ABCD)'$ ii) $Y=[D(A+BC)]'$	[5+5]
6.a)	Explain different capacitances present in CMOS design.	[5+5]
b)	Explain the concept of MOSFET as switches with suitable example.	
	OR	
7.	Write short notes on: a) Ratioed Circuits b) Dynamic Circuits.	[5+5]

8.a) Explain the operation of a basic 4 bit adder.
b) Explain the operation of booth multiplication with suitable example. [5+5]

OR

9.a) Design a 1:16 demultiplexer using 1:8 demultiplexers.
b) Draw the structure of a 4×4 static RAM and explain it's operation. [5+5]

10.a) Discuss any two types of programming technology used in FPGA design.
b) Explain ATPG fault models. [5+5]

OR

11.a) What is programmable devices? How it differs from ROM?
b) Explain fault models of VLSI Design. [5+5]

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