R09

Code No: C5702

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, October - 2015

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

(VLSI System Design/VLSI Design)

Time: 3hours **Max.Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) Compare in terms of speed and in system programmability of lattice PLSI's architecture and CYPRES FLASH 370.

b) Describe Altera's MAX 7000 PLD with the help of logical array block and Macro cell Diagrams. [6+6]

2.a) Discuss the design structure of AT&Ts optimized reconfigurable cell arrays.

b) Explain the routing architecture of an ACTEL FPGA and give the speed performance of ACTEL-ACT-1,2,3. [6+6]

3.a) Draw and discuss logic blocks of FPGAs.

b) With the help of neat sketches describe ALTERA's FLEX logic 8000 series. [6+6]

4.a) Write about one-hot state machine design method.

b) Discuss the properties of petrinetes for state machine. [6+6]

5.a) List out the salient features of mentor graphics EDA tool "FPGA advantage".

b) Write about the design flow using FPGAs. [6+6]

6.a) Explain the design flow for parallel adders and parallel controllers using mentor graphics EDA tool.

b) Write briefly about Linked state machines. [6+6]

7.a) Explain about the technology mapping for FPGAs.

b) Explain about front end digital design tools for FPGAs and ASICs. [6+6]

8.a) Write the features of Altera FLEX logic-10000 SERIES CPLD.

b) Write the Applications of CPLD and FPGAs in digital design. [6+6]

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