Code No: 53024 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year I Semester Examinations, December-2014
DIGITAL LOGIC DESIGN
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Explain BCD codes, Excess-3 code, Gray code, and ASCII codes used in digital systems and write the codes for decimal numbers 0-9 in each of these codes.
b) Write about error detecting codes and error correcting codes used in digital systems.
c) i) Convert $68BE_{16}$ to Binary and then Octal
ii) Convert 345_{10} to binary and Hexadecimal.

2.a) What are Minterms and Maxterms? Write the minterms and maxterms for three binary variables and express the Boolean function $F = A + B'C$ in sum of minterms.
b) Describe the Characteristics of various digital logic families.
c) Convert $(AB + C)(B + C'D)$ expression into sum of products and product of sums form.

3.a) Explain the methods of minimization of Boolean functions using four variable Karnaugh map and simplify the Boolean function
F(A, B, C, D) = $\sum$(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14).
b) Implement the following Boolean function using NAND gates and NOR gates after simplification using map method: $F(x, y, z) = (1, 2, 3, 4, 5, 7)$.

4.a) Draw the logic diagram of a 4-bit adder subtractor and explain its operation by taking suitable examples.
b) Explain the functions of multiplexers and decoders in digital logic design and draw the logic diagram of 4 to1 line multiplexer.

5.a) Draw the logic diagram of sequence detector with D-flip-flops and explain its operation with help of state table and state diagrams.
b) Design a logic diagram for a 3-bit binary counter using T-flip-flops. Write its state table, state diagram and the HDL description of the circuit.

6.a) Draw the circuit diagram of a 4-bit UP/DOWN binary counter and explain its working with the help of its state diagram.
b) Write the HDL behavioral and structural description of 4-bit universal shift register.

7.a) What are PLAs? Explain the functions and applications of PLAs in memory addressing and implement the following two Boolean functions with a PLA:
$F_1(A, B, C) = \sum(0, 1, 2, 4)$
$F_2(A, B, C) = \sum(0, 5, 6, 7)$
b) Draw the block diagram of general CPLD configuration and explain its working and compare the performance of CPLD with FPGA.

8.a) Explain the working of an Asynchronous sequential circuit and its analysis procedure with the help of necessary circuits , maps and tables.

b) Explain the Hazards in combinational circuits and their removal in AND-OR circuit and NAND circuit.

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