

## II B.Tech I Semester Examinations, May/June 2012

## PULSE AND DIGITAL CIRCUITS

Common to Electronics And Telematics, Electronics And Instrumentation Engineering, Electronics And Communication Engineering, Electrical And Electronics Engineering

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Define the following for a Transistor switch.
  - i. Rise time.
  - ii. Fall time.
  - iii. Storage Time.
  - iv. Delay time.
- (b) Give the expression for rise-time and fall-time in terms of transistor parameters and operating currents. [8+8]
2. (a) Derive the expression for rise time of integrating circuit and prove that it is proportional to time constant and inversely proportional to upper 3 dB frequency.
- (b) Explain the operation of RC low pass circuit when exponential input is applied. [8+8]
3. (a) Draw and explain a sampling diode whose response is not sensitive to the upper level of the control voltage.
- (b) Draw and explain a unidirectional gate which delivers an output only at a coincidence of a number of control voltages. [8+8]
4. (a) Draw and clearly indicate the restoration time and flyback time on the typical waveform of a time base voltage.
- (b) Derive the relation between the slope, transmission and displacement errors
- (c) Explain how UJT is used in a sweep circuit? [6+4+6]
5. (a) Determine  $V_o$  for the network shown in figure 5a for the given waveform. Assume ideal Diodes.

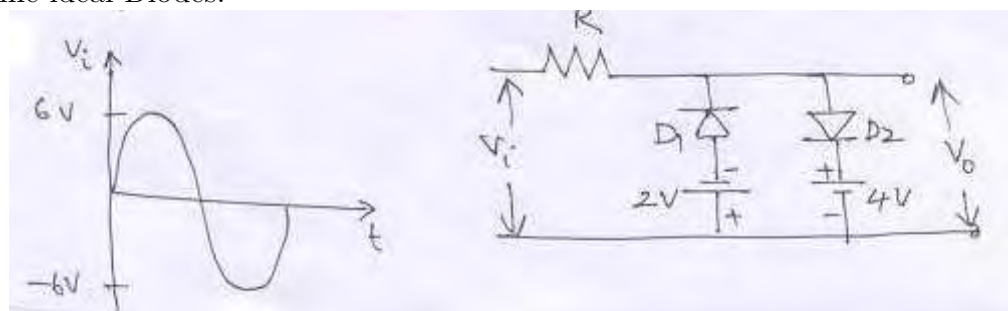


Figure 5a

- (b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation. [8+8]
6. (a) What are the basic logic gates which perform almost all the operations in Digital communication systems?  
(b) Give some applications of logic gates.  
(c) Define a positive and negative logic systems.  
(d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system. [4+4+4+4]
7. (a) What do you mean by a relaxation circuit? Give a few examples of relaxation circuits.  
(b) With the help of neat waveforms, explain sine wave frequency division with a sweep circuit. [8+8]
8. (a) Design a Schmitt trigger circuit NPN silicon transistors to meet the following specifications.  $V_{CC} = 12V$ ,  $UTP = 4V$ ,  $LTP = 2V$ ,  $h_{FE} = 60$ ,  $I_{C_2} = 3 \mu A$ . Use relevant assumptions and the empirical relationships.  
(b) Give the Applications of Schmitt trigger. [12+4]

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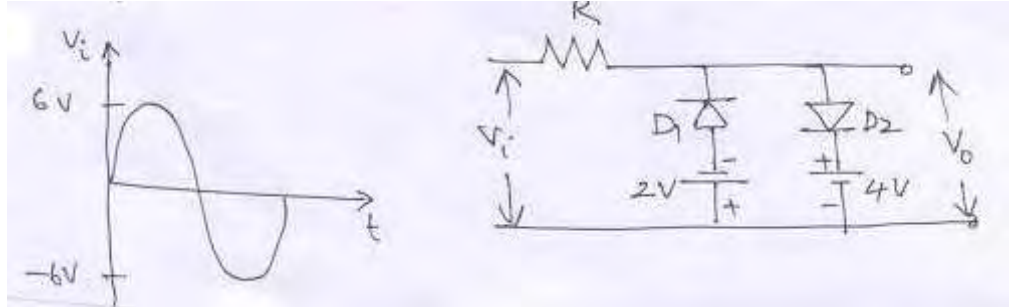


Figure 5a

- (b) Draw the basic circuit diagram of positive peak clamper circuit and explain its operation. [8+8]
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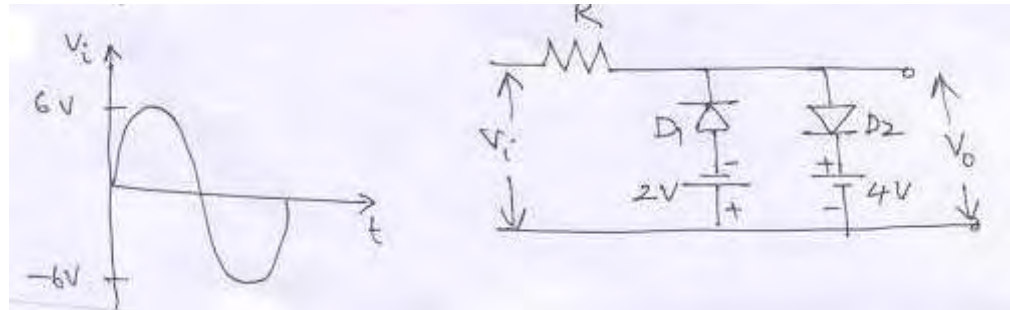


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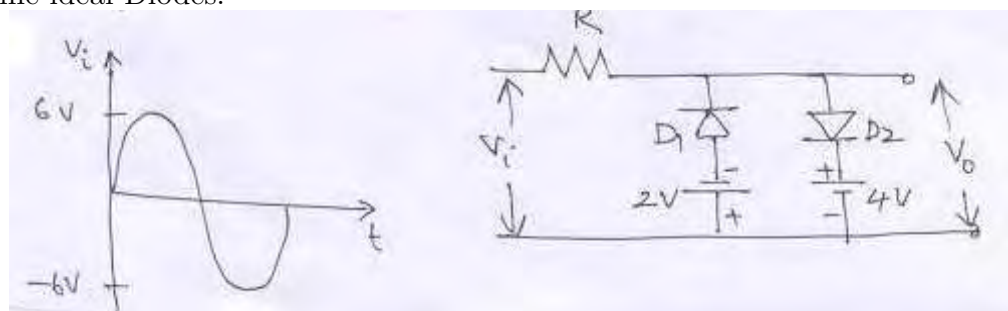


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