Code No: 07A4EC13 **R07** **Set No. 2**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Give the typical horizontal and vertical microinstruction formats. [8]
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]

2. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices. [4+4+4+4]

3. What is cache coherence? Explain different solutions to the cache coherence problem. [16]

4. . Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]

5. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]

6. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity?. What is odd function and even function?. To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F. [16]

7. (a) What are the relative advantages of ones complement and two's complement methods.
   (b) Explain subtraction procedure using complement representation. [8+8]

8. Explain the following:
   (a) Magnetic Tape Systems
   (b) Optical Disc
   (c) DVD Technology. [5+5+6]

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Code No: 07A4EC13 **R07** **Set No. 4**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. . Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]

2. (a) Give the typical horizontal and vertical microinstruction formats. [8]
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]

3. Explain the following:
   (a) Magnetic Tape Systems
   (b) Optical Disc
   (c) DVD Technology. [5+5+6]

4. What is cache coherence? Explain different solutions to the cache coherence problem. [16]

5. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices. [4+4+4+4]

6. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity?. What is odd function and even function?. To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F. [16]

7. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]

8. (a) What are the relative advantages of ones complement and two's complement methods.
   (b) Explain subtraction procedure using complement representation. [8+8]

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Code No: 07A4EC13 **R07** **Set No. 1**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. . Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]

2. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity?. What is odd function and even function?. To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F. [16]

3. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]

4. What is cache coherence? Explain different solutions to the cache coherence problem. [16]

5. (a) What are the relative advantages of ones complement and two's complement methods.
   (b) Explain subtraction procedure using complement representation. [8+8]

6. Explain the following:
   (a) Magnetic Tape Systems
   (b) Optical Disc
   (c) DVD Technology. [5+5+6]

7. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices. [4+4+4+4]

8. (a) Give the typical horizontal and vertical microinstruction formats. [8]
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]

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Code No: 07A4EC13 **R07** **Set No. 3**

II B.Tech II Semester Examinations,April/May 2012
COMPUTER ORGANIZATION
Common to IT, ICE, E.COMP.E, CSE, CSSE

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. What is cache coherence? Explain different solutions to the cache coherence problem. [16]

2. (a) Explain array processors in detail.
   (b) Explain Vector Processing. [8+8]

3. (a) What are the relative advantages of ones complement and two's complement methods.
   (b) Explain subtraction procedure using complement representation. [8+8]

4. Explain the following:
   (a) Magnetic Tape Systems
   (b) Optical Disc
   (c) DVD Technology. [5+5+6]

5. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity?. What is odd function and even function?. To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F. [16]

6. . Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]

7. (a) Give the typical horizontal and vertical microinstruction formats. [8]
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]

8. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices. [4+4+4+4]

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