Code No: 07A4EC02 **R07** **Set No. 2**

II B.Tech II Semester Examinations,April/May 2012
LINEAR AND DIGITAL IC APPLICATIONS
Common to Instrumentation And Control Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With help of a block diagram explain the basic building blocks of an Op-amp.
   (b) What does the term 'balanced output' mean in an Op-amp?
   (c) List the parameters that should be considered for AC and DC applications. [6+2+8]

2. (a) What is all pass filter? Explain.
   (b) Design a narrow band pass filter using one Op-Amp. The resonant frequency is 128 Hz and Q=1.5. Select C = 0.1 μF. [8+8]

3. (a) The basic step of a 16-bit DAC is 10.3 mV. If 0000000000000000 represents 0V, what output is produced if the input is 1101101111111111?
   (b) Calculate the values of the LSB, MSB and full scale output for an 32 bit DAC for the 0 to 20V. [8+8]

4. (a) Explain the terms Lock range, Capture range and Pull-in time of a PLL. How are Lock Range and Capture range determined?
   (b) Design a PLL circuit using IC 565 to get
      i. Free-running frequency = 4.5 KHz.
      ii. Lock range of 2 KHz and
      iii. Capture range = 100 Hz.

      Assume a supply voltage of $\pm$ or - 10V. Show the circuit diagram with all component values. [8+8]

5. Convert the decimal numbers to gray codes using Ex- OR gates
   (a) 98
   (b) 27 [8+8]

6. (a) Define transmission gate
   (b) Design and explain the working of transmission gate using CMOS. [8+8]

7. (a) Compare synchronous & Asynchronous circuits.
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [8+8]

8. (a) Explain the non-linear application of Op-amp as logarithmic and anti logarithmic amplifier.

(b) Design an Integrator to integrate an I/P signal that varies in frequency from 1 KHz to 10 KHz and plot the O/P wave forms if the I/P is a sine wave of 1V peak at 1 KHz. [10+6]

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Code No: 07A4EC02 **R07** **Set No. 4**

II B.Tech II Semester Examinations,April/May 2012
LINEAR AND DIGITAL IC APPLICATIONS
Common to Instrumentation And Control Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Compare synchronous & Asynchronous circuits.
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [8+8]
2. (a) Explain the non-linear application of Op-amp as logarithmic and anti logarithmic amplifier.
   (b) Design an Integrator to integrate an I/P signal that varies in frequency from 1 KHz to 10 KHz and plot the O/P wave forms if the I/P is a sine wave of 1V peak at 1 KHz. [10+6]
3. (a) Explain the terms Lock range, Capture range and Pull-in time of a PLL. How are Lock Range and Capture range determined?
   (b) Design a PLL circuit using IC 565 to get
      i. Free-running frequency = 4.5 KHz.
      ii. Lock range of 2 KHz and
      iii. Capture range = 100 Hz.

   Assume a supply voltage of ± or - 10V. Show the circuit diagram with all component values. [8+8]
4. (a) What is all pass filter? Explain.
   (b) Design a narrow band pass filter using one Op-Amp. The resonant frequency is 128 Hz and Q=1.5. Select C = 0.1 μF. [8+8]
5. Convert the decimal numbers to gray codes using Ex- OR gates
   (a) 98
   (b) 27 [8+8]
6. (a) The basic step of a 16-bit DAC is 10.3 mV. If 0000000000000000 represents 0V, what output is produced if the input is 1101101111111111?
   (b) Calculate the values of the LSB, MSB and full scale output for an 32 bit DAC for the 0 to 20V. [8+8]
7. (a) Define transmission gate
   (b) Design and explain the working of transmission gate using CMOS. [8+8]
8. (a) With help of a block diagram explain the basic building blocks of an Op-amp.

(b) What does the term 'balanced output' mean in an Op-amp?

(c) List the parameters that should be considered for AC and DC applications.

[6+2+8]

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Code No: 07A4EC02 **R07** **Set No. 1**

II B.Tech II Semester Examinations,April/May 2012
LINEAR AND DIGITAL IC APPLICATIONS
Common to Instrumentation And Control Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is all pass filter? Explain.
   (b) Design a narrow band pass filter using one Op-Amp. The resonant frequency is 128 Hz and Q=1.5. Select C = 0.1 μF. [8+8]
2. (a) Explain the non-linear application of Op-amp as logarithmic and anti logarithmic amplifier.
   (b) Design an Integrator to integrate an I/P signal that varies in frequency from 1 KHz to 10 KHz and plot the O/P wave forms if the I/P is a sine wave of 1V peak at 1 KHz. [10+6]
3. (a) Compare synchronous & Asynchronous circuits.
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [8+8]
4. (a) The basic step of a 16-bit DAC is 10.3 mV. If 0000000000000000 represents 0V, what output is produced if the input is 1101101111111111?
   (b) Calculate the values of the LSB, MSB and full scale output for an 32 bit DAC for the 0 to 20V. [8+8]
5. Convert the decimal numbers to gray codes using Ex- OR gates
   (a) 98
   (b) 27 [8+8]
6. (a) Define transmission gate
   (b) Design and explain the working of transmission gate using CMOS. [8+8]
7. (a) Explain the terms Lock range, Capture range and Pull-in time of a PLL. How are Lock Range and Capture range determined?
   (b) Design a PLL circuit using IC 565 to get
      i. Free-running frequency = 4.5 KHz.
      ii. Lock range of 2 KHz and
      iii. Capture range = 100 Hz.

      Assume a supply voltage of ± or - 10V. Show the circuit diagram with all component values. [8+8]
8. (a) With help of a block diagram explain the basic building blocks of an Op-amp.

(b) What does the term 'balanced output' mean in an Op-amp?

(c) List the parameters that should be considered for AC and DC applications.

[6+2+8]

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Code No: 07A4EC02 **R07** **Set No. 3**

II B.Tech II Semester Examinations,April/May 2012
LINEAR AND DIGITAL IC APPLICATIONS
Common to Instrumentation And Control Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With help of a block diagram explain the basic building blocks of an Op-amp.
   (b) What does the term 'balanced output' mean in an Op-amp?
   (c) List the parameters that should be considered for AC and DC applications. [6+2+8]

2. Convert the decimal numbers to gray codes using Ex- OR gates
   (a) 98
   (b) 27 [8+8]

3. (a) Explain the terms Lock range, Capture range and Pull-in time of a PLL. How are Lock Range and Capture range determined?
   (b) Design a PLL circuit using IC 565 to get
      i. Free-running frequency = 4.5 KHz.
      ii. Lock range of 2 KHz and
      iii. Capture range = 100 Hz.

   Assume a supply voltage of ± or - 10V. Show the circuit diagram with all component values. [8+8]

4. (a) Compare synchronous & Asynchronous circuits.
   (b) Design a Mod-6 synchronous counter using J-K flip flops. [8+8]

5. (a) The basic step of a 16-bit DAC is 10.3 mV. If 0000000000000000 represents 0V, what output is produced if the input is 1101101111111111?
   (b) Calculate the values of the LSB, MSB and full scale output for an 32 bit DAC for the 0 to 20V. [8+8]

6. (a) Explain the non-linear application of Op-amp as logarithmic and anti logarithmic amplifier.
   (b) Design an Integrator to integrate an I/P signal that varies in frequency from 1 KHz to 10 KHz and plot the O/P wave forms if the I/P is a sine wave of 1V peak at 1 KHz. [10+6]

7. (a) Define transmission gate
   (b) Design and explain the working of transmission gate using CMOS. [8+8]

8. (a) What is all pass filter? Explain.

   (b) Design a narrow band pass filter using one Op-Amp. The resonant frequency is 128 Hz and Q=1.5. Select C = 0.1 μF. [8+8]

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