Code No: 07A3EC16 **R07** **Set No. 2**

II B.Tech I Semester Examinations,May/June 2012
DIGITAL LOGIC DESIGN
Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain about Error detection and Correction in detail? [16]
2. (a) Implement Half adder using 4 NAND gates
   (b) Implement full subtrctor using NAND gates only. [6+10]
3. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.
   (b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open.The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x
   Mr.B has keys for locks v& y
   Mr.C has keys for locks w& y
   Mr.D has keys for locks x& z
   Mr.E has keys for locks v& z
      i. Determine the minimal no. of executives required to open the safe.
      ii. Find all the combinations of executives that can open the safe, write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are present
      iii. Who is the 'essential executive' without whom the safe cannot be opened? [7+9]
4. Write an HDL behavioral description of the JK flip-flop using an if-else statement based on the value of the Present state (Hint: consider the characteristic equation When Q=0 or Q=1) [16]
5. Explain about the Following
   (a) Serial Transfer in 4-bit shift Registers
   (b) Binary Ripple Counter
   (c) HDL for Synchronous Counter. [16]
6. Implement 8421 BCD subtraction using 9's complement and full adder chip and few other gates. [16]
7. What are the Procedural steps involved in designing an asynchronous Sequential circuit? Briefly explain them. [16]

8. Convert the following numbers:
   (a) 10101100111.0101 to Base 10
   (b) $(153.513)_{10} = (\ )_8$
   (c) Find $(3250 - 72532)_{10}$ using 10's complement
   (d) Divide 01100100 by 00011001
   (e) Given that (292)10 =$(1204)_b$ determine 'b' [3+4+3+3+3]

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Code No: 07A3EC16 **R07** **Set No. 4**

II B.Tech I Semester Examinations,May/June 2012
DIGITAL LOGIC DESIGN
Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Write an HDL behavioral description of the JK flip-flop using an if-else statement based on the value of the Present state (Hint: consider the characteristic equation When Q=0 or Q=1) [16]
2. Explain about Error detection and Correction in detail? [16]
3. Implement 8421 BCD subtraction using 9's complement and full adder chip and few other gates. [16]
4. Explain about the Following
   (a) Serial Transfer in 4-bit shift Registers
   (b) Binary Ripple Counter
   (c) HDL for Synchronous Counter. [16]
5. (a) Implement Half adder using 4 NAND gates
   (b) Implement full subtrctor using NAND gates only. [6+10]
6. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.
   (b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open.The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x
   Mr.B has keys for locks v& y
   Mr.C has keys for locks w& y
   Mr.D has keys for locks x& z
   Mr.E has keys for locks v& z
      i. Determine the minimal no. of executives required to open the safe.
      ii. Find all the combinations of executives that can open the safe, write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are present
      iii. Who is the 'essential executive' without whom the safe cannot be opened? [7+9]
7. Convert the following numbers:

(a) 10101100111.0101 to Base 10

(b) $(153.513)_{10} = (\ )_8$

(c) Find $(3250 - 72532)_{10}$ using 10's complement

(d) Divide 01100100 by 00011001

(e) Given that (292)10 $=(1204)_b$ determine 'b' [3+4+3+3+3]

8. What are the Procedural steps involved in designing an asynchronous Sequential circuit? Briefly explain them. [16]

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Code No: 07A3EC16 **R07** **Set No. 1**

II B.Tech I Semester Examinations,May/June 2012
DIGITAL LOGIC DESIGN
Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering
Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.
   (b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open.The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x
   Mr.B has keys for locks v& y
   Mr.C has keys for locks w& y
   Mr.D has keys for locks x& z
   Mr.E has keys for locks v& z
      i. Determine the minimal no. of executives required to open the safe.
      ii. Find all the combinations of executives that can open the safe, write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are present
      iii. Who is the 'essential executive' without whom the safe cannot be opened? [7+9]

2. Convert the following numbers:
   (a) 10101100111.0101 to Base 10
   (b) $(153.513)_{10} = (\ )_8$
   (c) Find $(3250 - 72532)_{10}$ using 10's complement
   (d) Divide 01100100 by 00011001
   (e) Given that $(292)10 = (1204)_b$ determine 'b' [3+4+3+3+3]

3. (a) Implement Half adder using 4 NAND gates
   (b) Implement full subtrctor using NAND gates only. [6+10]

4. Explain about Error detection and Correction in detail? [16]

5. Explain about the Following
   (a) Serial Transfer in 4-bit shift Registers
   (b) Binary Ripple Counter
   (c) HDL for Synchronous Counter. [16]

6. Write an HDL behavioral description of the JK flip-flop using an if-else statement based on the value of the Present state (Hint: consider the characteristic equation When Q=0 or Q=1) [16]

7. What are the Procedural steps involved in designing an asynchronous Sequential circuit? Briefly explain them. [16]

8. Implement 8421 BCD subtraction using 9's complement and full adder chip and few other gates. [16]

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Code No: 07A3EC16 **R07** **Set No. 3**

II B.Tech I Semester Examinations,May/June 2012
DIGITAL LOGIC DESIGN
Common to Information Technology, Computer Science And Engineering, Computer Science And Systems Engineering
Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Implement 8421 BCD subtraction using 9's complement and full adder chip and few other gates. [16]

2. Convert the following numbers:
   (a) 10101100111.0101 to Base 10
   (b) $(153.513)_{10} = (\ )_8$
   (c) Find $(3250 - 72532)_{10}$ using 10's complement
   (d) Divide 01100100 by 00011001
   (e) Given that (292)10 =$(1204)_b$ determine 'b' [3+4+3+3+3]

3. (a) Implement Half adder using 4 NAND gates
   (b) Implement full subtrctor using NAND gates only. [6+10]

4. (a) Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7.
   (b) A safe has 5 locks:v,w,x,y,all of which must be unlocked for the safe to open.The keys to the locks are distributed among five executives in the following manner: Mr.A has keys for locks v& x
   Mr.B has keys for locks v& y
   Mr.C has keys for locks w& y
   Mr.D has keys for locks x& z
   Mr.E has keys for locks v& z
      i. Determine the minimal no. of executives required to open the safe.
      ii. Find all the combinations of executives that can open the safe, write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are present
      iii. Who is the 'essential executive' without whom the safe cannot be opened? [7+9]

5. Explain about the Following
   (a) Serial Transfer in 4-bit shift Registers
   (b) Binary Ripple Counter

(c) HDL for Synchronous Counter. [16]

6. Write an HDL behavioral description of the JK flip-flop using an if-else statement based on the value of the Present state (Hint: consider the characteristic equation When Q=0 or Q=1) [16]

7. What are the Procedural steps involved in designing an asynchronous Sequential circuit? Briefly explain them. [16]

8. Explain about Error detection and Correction in detail? [16]

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