R13

Code No: 126EN

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, May - 2017

VLSI DESIGN

(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	What are the advantages of BiCMOS process compare with the CMOS.	[2]
b)	List the fabrication procedures for IC Technologies.	[3]
c)	Draw the VLSI Design Flow.	[2]
d)	Draw the stick diagram for two inputs NOR gate.	[3]
e)	What is switch logic?	[2]
f)	What are the issues involved in driving large capacitive loads in VLSI circuits.	[3]
g)	Design a 2-bit Parity generator.	[2]
h)	What is Booth's algorithm?	[3]
i)	Write the Comparison between FPGA and CPLD.	[2]
j)	What type of faults can be reduced by improving layout design?	[3]

PART - B

(50 Marks)

2.a) Discuss the Basic Electrical Properties of MOS and BiCMOS Circuits.
b) Derive the expression for estimation of Pull-Up to Pull-Down ratio of an n-MOS inverter driven by another n-MOS inverter. [5+5]

OR

3.a) Derive the relationship between I_{ds} and V_{ds}
b) Derive the expression for transfer characteristics of CMOS Inverter. [5+5]

4.a) Explain in detail about the scaling concept in VLSI circuit Design.
b) Draw the Layout Diagrams for NAND Gate using nMOS. [5+5]

OR

5.a) Explain λ-based Design Rules in VLSI circuit Design.
b) Draw the Layout Diagrams for CMOS Inverter. [5+5]

6. Explain the following:
a) Fan-in
b) Fan-out
c) Choice of layers. [10]

OR

7. Describe the following:
a) Pseudo-nMOS Logic
b) Domino Logic. [5+5]

8.a) Draw the schematic and logic diagram for a single bit adder and explain its operation with truth table.

b) With neat circuit diagram, explain the operation of Barrel shifter. [5+5]

OR

9.a) Explain about Serial access memories.

b) Explain about design of an ALU subsystem in brief. [5+5]

10.a) Explain Architecture of FPGA in detail.

b) What are the draw backs of PLAs? How PLAs are used to implement combinational and sequential logic circuits? [5+5]

OR

11.a) Why stuck-at faults occur in CMOS circuits? Explain with suitable logical diagram.

b) Why the chip testing is needed? At what levels testing a chip can occur? [5+5]

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