R09

Code No: 53024

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2017
DIGITAL LOGIC DESIGN
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Solve for x
i) $(257)_8 = (x)_2$
ii) $(21.625)_{10} = (x)_8$
iii) $(BC.2)_{16} = (x)_8$
iv) $(33)_{10} = (201)_x$
b) Express the Decimal Digits 0-9 in BCD, 2421, 84-2-1 and Excess-3. [8+7]

2.a) Simplify the following Boolean expressions using the Boolean theorems.
i)(A+B+C) (B′+C) + (A+D) (A′+C) ii) (A+B) (A+B′) (A′+B).
b) Why a NAND and NOR gates are known as universal gates? Simulate all the logical operations using NAND and NOR gate. [8+7]

3.a) Minimize the following expressions using K-map and realize using NAND Gates.
$f = \sum m(0,1,4,5,6,7,9,11,15) + d(10,14)$
b) Minimize the following expression using K-map and realize using NOR Gates.
$f = \prod M(1,4,5,11,12,14) \cdot d(6,7,15)$. [8+7]

4.a) Describe the operations performed by the following logic circuits with an example:
i) Comparator ii) Decoder iii) Encoder.
b) Explain the operation of a 3-to-8 decoder 74LS138. Realize 4-to-16 decoder using two 3-to-8 decoders. [8+7]

5.a) Explain the realization of SR flip-flop, JK flip-flop using D flip-flop.
b) Explain the analysis of clocked sequential circuits in detail. [8+7]

6.a) Explain the differences between asynchronous and synchronous counters. Design a MOD-10 ripple counter.
b) Design and construct MOD-5 synchronous counter using JK flip-flops. [8+7]

7.a) Draw and explain the block diagram of PAL.
b) Explain in detail the SRAM and DRAM. [8+7]

8.a) What do you mean by hazard? Classify and explain.
b) Describe the cycles in asynchronous sequential circuits. [7+8]

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