Code No: X0524 **R07**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, March - 2017
DIGITAL LOGIC DESIGN
(Common to CSE, IT)

Time: 3 hours **Max. Marks: 80**

Answer any five questions
All questions carry equal marks

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1.a) Explain how BCD addition is carried out and perform the addition of following BCD numbers: i) 1001 and 0100 ii) 00011001 and 00010100.

b) Describe the floating point representation of numbers and determine the number of bits required to represent in floating point notation the exponent for decimal numbers in the range of $10^{\pm 86}$. [8+8]

2.a) Using demorgans theorem, convert the following Boolean expressions to equivalent expression so that have only OR and complement operations. Show that the functions can be implement with logic diagrams that have only OR gates and inverters

i) f= $\bar{x}y+\bar{x}z+\bar{y}z$

ii) f=$(y+\bar{z})(x+y)(\bar{y}+z)$

b) Express the following boolean function D=$(\bar{A}+B)(\bar{B}+C)$ as

i) POS form ii) SOP form. [8+8]

3.a) Simplify the following expression into sum of products using Karnaugh map. F(A,B,C,D) =$\sum$ (1,3,4,5,6,7,9,12, 13)

b) Find the minimal sum of products for the boolean expression f = $\sum$(1,2,3,7,8,9,10,11,14,15) using Quine-McCluskey method. [8+8]

4.a) Distinguish between encoder and decoder. Implement a full adder using IC74138.

b) Design a priority encoder for a system with a 3 inputs, the middle bit with highest priority encoding to 10, the MSB with next priority encoding to 11, while the LSB with least priority encoding to 01. [8+8]

5.a) Write the basic recommended steps for the design of a clocked synchronous sequential circuits.

b) With a suitable example explain Mealy and Moore model in a sequential circuit analysis. [8+8]

6.a) Explain a universal shift register with the help of logic diagram, mode control table.

b) Design a synchronous counter using JK flip-flops to count the sequence 0,1,2,4,5,6,0,1,2. [8+8]

7.a) List the PLA programming table and draw the PLA structure for the BCD-to-Excess-3-code converter.

b) Give the classification of memories. [4+12]

8 a) Find a circuit that has no static hazards and implements the Boolean function $F(A,B,C,D) = \Sigma\,(0,2,6,7,8,10,12)$

b) What are the steps for the design of asynchronous sequential circuit? [12+4]

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