R09

Code No: 09A70412

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year I Semester Examinations, June/July-2014

VLSI DESIGN

(Common to ECE, EIE, BME, IT, ETM, ECM, ICE)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

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1.a) List the fabrication procedures for IC Technologies.
b) What are the masks involved in PMOS design, Show with all necessary sketches.

2.a) Derive the expression for estimation of Pull-Up to Pull-Down ratio of an n-MOS inverter driven by another n-MOS inverter.
b) Explain the operation of BiCMOS inverter with improved versions.

3.a) Explain the stick diagrams design Rules and layout.
b) Design a Stick Diagram for 2-input nMOS NAND and NOR gates.

4.a) Explain 2×1 Multiplexer using transmission gate and tri-state inverter.
b) Explain the following:
i) Fan-in
ii) Fan-out
iii) Choice of layers
iv) Capacitive load

5.a) What are the data path operators? Give its significance.
b) Explain bit serial adder implementation.
c) Discuss Array shifting using transmission gate.

6.a) Explain the operation of SRAM cell with its construction.
b) Write a brief notes on Serial Access Memories.

7.a) Write the Comparison between FPGA & CPLD.
b) Explain PLA Architecture with an example.

8.a) Explain the need of Boundary Scan.
b) Explain the Following:
i) Fault Simulation
ii) Observability
iii) Controllability
iv) Stuck-at-fault Model.

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