Code No: A5711 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech. I SEMESTER EXAMINATIONS, APRIL/MAY-2012
MODELING AND SYNTHESIS WITH VERILOG HDL
(VLSI SYSTEM DESIGN)

Time: 3 hours **Max. Marks.60**

Answer any Five Questions
All questions carry equal marks

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1. Explain the explicit and implicit structural descriptions using examples.

2. Describe inertial delay and transport delay using an example.

3. Explain the four looping mechanisms in Verilog that allow procedural statements to be executed repeatedly within an activity flow.

4. (a) Explain the syntax and rules for tasks and functions in Verilog.
   (b) Explain the synthesis of three-state buffers.

5. Explain how a combinational logic circuit can be synthesized from a netlist of gate-level Verilog primitives.

6. (a) Discuss why switch-level modeling is useful.
   (b) Explain the Verilog model of a three-input static CMOS NAND gate with the help of a diagram.

7. (a) Explain the organisation of procedural constructs in Verilog.
   (b) Explain the synthesis of Non-blocking procedural assignments.

8. Write short notes on any two of the following:
   (a) Synthesis of relational and identity operators
   (b) Disable statement and fork…join statement
   (c) Benefits of HDL based designs

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