L&B

R09

Code No: 09A60502

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech III Year II Semester Examinations, May/June, 2013
VLSI Design
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Compare the performance of various oxidation process.
b) Compare MOS and CMOS and Bi-CMOS technologies. [15]

2. Explain the working of Bi-CMOS inverter using appropriate transfer characteristics. [15]

3.a) Explain the different types of contact cuts used in CMOS design and fabrication.
b) Draw the stick diagram layout of an 8:1 inverter using appropriate transfer characteristics. [15]

4. Explain CMOS domino logic circuit with an example. Compare its performance over that of CMOS logic. [15]

5. Design a 4-bit synchronous up/down counters using adders and registers. Implement an adder cell and a register cell using transmission gates and explain. [15]

6.a) Discuss the need of stick diagrams and explain with a example.
b) Explain the need for low power design circuits in VLSI chip fabrication. [15]

7. Illustrate the simultaneous minimization of three functions.
$f_1(A,B,C,D) = \sum_m(0,2,7,10) + d(12,15)$
$f_2(A,B,C,D) = \sum_m(2,4,5) + d(6,7,8,10)$
$f_3(A,B,C,D) = \sum_m(2,7,8) + d(0,5,13)$ and implement using suitable PAL. [15]

8. What is fault simulation? Explain briefly fault models. Explain the various stuck at fault models with suitable examples. [15]

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