R16

Code No: 137JD

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year I Semester Examinations, December - 2019

VLSI DESIGN

(Common to ECE, EIE)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) Write the equation for threshold voltage in terms of fabrication parameters. [2]
b) What is latchup? How to reduce it? [3]
c) What are the different MOS layers? [2]
d) Draw the layout for nMOS inverter. [3]
e) How to choose layers? [2]
f) What is mean by fan-in and fan-out? [3]
g) Draw the circuit diagram of one transistor DRAM. [2]
h) What are the advantages of serial access memories? [3]
i) Why low power VLSI circuits are needed? [2]
j) Compare PLAs and PALs. [3]

PART – B

(50 Marks)

2.a) Explain the fabrication steps of CMOS n-well process with neat diagrams.
b) Identify the different regions on the V_{ds} vs. I_{ds} characteristics and explain it. [6+4]

OR

3.a) What are the different pull ups used in VLSI design? Explain them.
b) What will happen if logical one is applied on the BiCMOS inverter? Explain it with neat circuit diagram. [5+5]

4.a) Explain the process at each stage of VLSI design flow.
b) Draw the stick diagram for NAND gate and explain it. [5+5]

OR

5.a) What are the different design rules? Write them.
b) What is scaling? How to scale the different design parameters? [5+5]

6.a) What is dynamic logic? Explain its basic gate functionality.
b) How to calculate the delay due inductance in the VLSI circuits? Explain. [4+6]

OR

7.a) What are the different complex logic gates and compare their performance in all aspects.
b) What is wiring capacitance? How to calculate it in the design of VLSI? [5+5]

8. Design a decade counter and draw its logic and circuit diagram and also write how to improve its performance in VLSI applications? [10]

OR

9. Draw a six transistor RAM circuit and explain its working and also write its merits and demerits. [10]

10.a) What is FPGA an draw its structure and also write its advantages.
b) Explain different design strategies for testing a VLSI circuit. [5+5]

OR

11.a) What is principle of testing CMOS circuit? Explain any one procedure for it.
b) Design the following function using PALs:
$Y=x'y'w+z'w'+xz$ [5+5]

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