Code No: 153AB **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, December - 2019

ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) What is mean by avalanche break down? [2]
b) What is the significance of operating point? [2]
c) Implement the AND gate using TTL logic. [2]
d) Write the any two basic theorems of Boolean algebra. [2]
e) Draw the 2×1 Multiplexer. [2]
f) Why filter is needed in rectifiers? Name some such filters. [3]
g) Compare CB and CC Configurations. [3]
h) Differentiate between DTL and modified DTL logic. [3]
i) Write the logic of full adder with Boolean equations. [3]
j) Define D flip-flop with the help of its characteristic equation. [3]

PART – B

(50 Marks)

2.a) Explain the operation of silicon p-n junction diode and obtain the forward bias and reverse bias Volt-Ampere characteristics.
b) How diode is used as a switch and define all switching times? [5+5]

OR

3.a) Draw any one of clipping circuit and explain its operation with suitable waveforms.
b) Explain the working of a full-wave rectifier and derive the expression for ripple factor. [5+5]

4.a) Explain compensation techniques with respect to BJT Biasing.
b) Draw and explain about multi stage CE amplifier. [5+5]

OR

5.a) Discuss about the nature of transistor at low frequencies.
b) Write the differences between BJT & JFET. [5+5]

6.a) Explain in detail how FET can be used as an amplifier.
b) Draw and explain CD amplifier with suitable diagrams. [5+5]

OR

7.a) Design a NAND gate in DTL logic and explain its operation with truth table.
b) What is totem pole? How it is used in TTL gates? [5+5]

8.a) Simplify the following function using Map method
$F(A,B,C,D)= \Sigma(0,1,2,3,4,6,9,10)+d(7,11,12,13,15)$.
b) Design a BCD to Excess-3 code converter. [5+5]

OR

9.a) Explain the functions of multiplexers and decoders in digital logic design and draw the logic diagram of 4 to1 line multiplexer.
b) Explain the working of 2-bit magnitude comparator. [5+5]

10.a) Distinguish between combinational and sequential switching circuits.
b) Draw the truth table of SR flip-flop and obtain its characteristic equation. [5+5]

OR

11.a) Explain in detail universal shift register with neat diagram.
b) Draw the logic diagram of a 4-bit ring counter using JK flip flops and explain its working. [5+5]

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