Code No: 126EN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, October/November - 2016
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define threshold voltage of a MOS device. [2]
b) What are pull-ups and write about the resistor pull-up and its usage. [3]
c) Explain about the contact cuts and approaches. [2]
d) Represent the Stick diagram of a NMOS inverter. [3]
e) Write about the clocked CMOS logic and its usage. [2]
f) Explain about the Wiring capacitance and its need. [3]
g) Mention about SRAM and its usage. [2]
h) Describe about the Serial Access Memories. [3]
i) Explain about the principle of Built in Self Test. [2]
j) Explain about test Principles used for testing. [3]

PART - B

(50 Marks)

2.a) Write about BiCMOS fabrication in a n-well process with a diagram.
b) Distinguish between Bipolar and CMOS devices technologies in brief. [5+5]

OR

3.a) Mention about the BICMOS Inverters and alternative BICMOS Inverters.
b) Determine the pull-up to pull down ratio for NMOS inverter driven by another NMOS Inverter. [5+5]

4.a) Discuss about the stick diagrams and their corresponding mask layout examples.
b) Draw the stick diagram of p-well CMOS inverter and explain the process. [5+5]

OR

5.a) Explain about the 2 μm CMOS Design rules and discuss with a layout example.
b) Draw and explain the layout for CMOS 2-input NAND gate. [5+5]

6. Discuss about the logics implemented in gate level design and explain the switch logic implementation for a four way multiplexer. [10]

OR

7.a) Describe about the methods for driving large capacitive loads.
b) Describe about the choice of fan – in and fan – out selection in gate level design. [5+5]

8.a) Design a shift register with the dynamic latch operated by a two-phase clock.

b) Explain the working principle of Ripple carry adder using Transmission Gates. [5+5]

OR

9.a) Explain about the Wallace tree multiplication and its design issues.

b) Draw the circuit diagram of four transistor DRAM cell with storage nodes. [5+5]

10.a) Explain the detailed logic configurable Block Architecture of FPGA.

b) Write a note on the different Parameters influencing low power design. [5+5]

OR

11. Explain the following in detail.

a) Chip level Test Techniques

b) Testability and practices. [5+5]

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