Code No: 5155N

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II Semester Examinations, April-2015
CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
(Embedded Systems)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 marks = 20

1.a) Draw and very briefly explain the macro-cell architecture of Max 7000 CPLD.
b) Briefly explain the functional logic implementation using LUT-based design in FPGAs.
c) What is the transition firing rule in petrinets?
d) Write the features of ACT3 architecture.
e) Design consideration of Digital PLLs using FPGAs.

PART - B

5 × 8 marks = 40

2. With neat figures explain the Architecture of Xilinx Cool Runner XCR3064XL CPLD. [8]

OR

3. Realize full adder circuit using:
a) PROM
b) PLA and
c) PAL. [2+3+3]

4. Explain how the design methodology and flows differ among different FPGA architectures. [8]

OR

5. Explain the design aspects of Altera's flex 8000 FPGA. [8]

6. Compare the Xilinx XC2000, XC3000 and XC4000 CLB and IOB Architectures. [8]

OR

7. Write notes on design tradeoff for SRAM based FPGAs architectures with regard to Density, Speed, Size and Routability. [8]

8. Implement a 6-bit loadable counter using ACT2 Architecture. [8]

OR

9.a) List the principles of programmable routing.
b) Write notes on routing architectures of Actel FPGAs. [4+4]

10. Explain general design issues and Implement a Fast DMA controller. [8]

OR

11. Write notes on A Position Tracker for a Robot Manipulator using FPGAs. [8]

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