A

Project Report

On

Implementation of LFSR Based Fast Error-Resilient Ternary Content Addressable Memory

Submitted in partial fulfilment of requirements for the award of the degree of

MASTER OF TECHNOLOGY

In

VLSI SYSTEM DESIGN

By

GADDAMEEDI KARUNAKAR

208R1D5705

Under the esteemed guidance of

Mr. Biroju Papachary

Associate Professor

Department of Electronics and Communication Engineering

CMR ENGINEERING COLLEGE

(UGC AUTONOMOUS)

(Approved by AICTE, NEW DELHI, Affiliated to JNTUH)

Kandlakoya, Medchal Road, R.R. Dist. Hyderabad-501401)

2021-22

CERTIFICATE

This is to certify that the dissertation entitled "**Implementation of LFSR Based Fast Error-Resilient Ternary Content Addressable Memory**" is being carried out by **GADDAMEEDI KARUNAKAR** bearing Roll Number **208R1D5705** in partial fulfilment of the academic requirements for the award of the degree of **MASTER OF TECHNOLOGY** in **VLSI SYSTEM DESIGN** for the year 2021-2022 submitted to the Department of ELECTRONICS AND COMMUNICATON ENGINEERING, CMR ENGINEERING COLLEGE, HYDERABAD.

Under the Guidance of

Mr. Biroju Papachary

Head of the Department

Dr. Suman mishra

External Examiner

DECLARATION

I hereby declare that the project entitled "**Implementation of LFSR Based Fast Error-Resilient Ternary Content Addressable Memory**" work done by me in campus at **CMR ENGINEERING COLLEGE**. Kandlakoya during the academic year 2021-2022 and is submitted as project in partial fulfillment of the award of degree of **MASTER OF TECHNOLOGY** in **VLSI SYSTEM DESIGN** from **JAWAHARLAL NEHRU TECHNOLOGY UNIVERSITY, HYDERABAD**

Gaddameedi Karunakar
(208R1D5705)

ACKNOWLEDGEMENT

A part from the efforts of me, the success of this seminar depends largely on the encouragement and guidelines of many others. I take this opportunity to express my gratitude to the people who have been instrumental in the successful completion of this seminar

I render my thanks to **Sri**. **CH. NARASIMHA REDDY**, Chairman CMR Engineering College**,** for his encouragement.

I express my sincere gratitude to **Dr. A.S REDDY,** Principal, CMR Engineering College**,** for providing excellent academic environment in the college.

I thank and express my gratitude to **Dr. SUMAN MISHRA,** Professor, Head ofthe Department**,** ECE for providing with both time and amenities to make this project a success within schedule

We take it a privilege to thank our project coordinator **Dr. S. POONGODI**, Professor, Department of ECE for her continuous guidance, support and unfailing patience throughout the project period.

I take unique privilege to express my thanks to supervisor **Mr.Biroju Papachary,** Associate Professor, Department of ECE, for his valuable guidance and encouragement given to me throughout this project

I extend my thanks to all the people, who have helped me a lot directly or indirectly in the completion of this project.

Gaddameedi Karunakar
(208R1D5705)

ABSTRACT

Memories are the major building blocks for various applications, which includes integrated circuits, digital circuits, digital equipment. The conventional memories are developed using Static Random Access Memory (SRAM) cells. However, they are facing the memory read-write synchronization issues, and stuck at faults with high errors. Therefore, this article is focused on implementation of Error-Resilient Ternary Content-Addressable Memory (ER-TCAM) for fast data storage with high speed read-write operations. Here, Linear Feedback Shift Register (LFSR)s were introduced for generating the random pattern sequences with address synchronization properties. Finally, LFSR based ER-TCAM provided the optimal data storage with high self-error detection, correction properties. The simulations revealed that the proposed method resulted in better area, delay, power performance as compared to conventional approaches.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES

LIST OF ABBREVATIONS

BIST	Built In Self-Test
CAM	Content Addressable Memory
CPU	Central Processing Unit
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
ERTCAM	Error Resilient Ternary Content Addressable Memory
FIFO	Fast In Fast Out
FPGAs	Field Programmable Gate Arrays
LFSR	Linear Feedback Shift Register
RAM	Random Access Memory
SRAM	Static Random Access Memory
TCAM	Ternary Content Addressable Memory

CHAPTER-1

INTRODUCTION

1.1 Overview of TCAM

Greater elements might well be connected to the single smart card, creating systems-on-a-chip (soc) with the many tricky devices some one existing design method. that whole scheduling anyway fast velocity world wide pulses must have alas be a key problem throughout process control as of universal correlation trying to scale was unable to continue to maintain this very same performance gains [1]. clock gating loops just need extra transmission line assets but instead pre - defined time from this. most contemporary technological devices have been using sequential described as follows, time or over time demand the availability of either a specific but instead firmly synced world - wide watch citation to any and every paragraph of transmission line. utilising self-timed but rather automated circuit design, that dearth a worldwide telegraphing reference voltage, is only one approach for dealing with both the watch propagation inherent problem. that whole industry's stubborn refusal to maneuver apart through the set up symmetric work flow and indeed the exclusion like reach maturity tools, however, have impeded this same soak up of other make necessary arrangements [2]. the alternative treatment plan was to use the the one worldwide synchronization smaller local symmetric (gals) [3] design approach versus concoct solution that combines full duplex styling methods. throughout this worldview, slabs were also formed to use conventional power make necessary arrangements, but these websockets buildings have been realtime for each other and must not transfer universal based on the established. even though it is often when easy to interrupt some one down the system up into multiple component pieces, this is infrequent that all of these components might operate autonomously. in consequence, transmitting data for both municipalities websockets slabs is critical. the primary problems through guys and girls aims to design seem to be confidently but rather effectually doing it too obligations.

Dual- Clock FIFO Design	Clock Requirement	Storage Elements	Clock haltable
Greenstreet[8]	Mesochronous	-	-
Chakraborty[9]	Require training time	-	-
Siezovic[10]	arbitrary	Linear	-
Chelcea[11]	arbitrary	Registers	-
Cummings	arbitrary	Memory array	No
This work	arbitrary	Memory array	yes

Table 1.1 Comparison of dual-clock FIFO designs.

a dual-clock first-input-first-output (FIFO) as well as mixed-clock first out is just one frame that really is and even more so likeminded for all this intent. two distinct counter receives also have to be housed through it modify the elemental png layout. each counter is used to data sources inhabiting its first out component, while another watch can then be used to data source choosing to leave its interface. info might well be dependably moved throughout all detach counter realms in the this ready - to - wear. instances once personal information was indeed shifted throughout all halts through counter domain controllers that just aren't completely adaptive but even so packages is one of side found in all parts like dual-clock FIFOs. as for positive integer periods after all halt between it farmer but rather end user, this same posited architectural style permit applications it and data transmission out all over devices that really are positioned out completely separate countdown hostnames. it's really incredibly helpful throughout software within which bandwidth, so instead of halt, is essential, like in many other digital signal initiatives.

Random obtain dram: exactly the sort memory chip which is well identified known as memory buffer (ram). though you may easily access another other memristive such as random - access memory for those who realize it and row a certain traverse at a certain compartment, bandwidth seems to be known as to have "random connect." through juxtaposition, random - access memory info may very well be recovered inside any series. here are the info that now the laptop uses or meets up with for all procedure. gets to drive, ordinarily this same hdd, are also used to data items.

But that said, such info should first be review into in the cognitive processing collection to ensure that its multicore to just use the others (ram).

Various kinds of ram random connectivity brain (SRAM) the new tech for use by static memory subsystem is so very distinction. evey recollection slightly through 6 GB of ram would be maintained together in slide connection. positive input data career and employment means it needs 5 to 6 discrete components and even some cables, and that never should be refreshed. in consequence, SRAM is just much faster just like energetic bandwidth. positive add meaning compartment, but even so, encompasses much more spatial on either a microprocessor than like a memory management compartment because it contents as much facets. resultantly, users can be less memory for each integrated circuits.

Each cell state such as static memory buffer had already various devices, generally four to seven, but its not a capacitance. stash is also its major objective. and thereby, whilst the diversity random access memory is less expensive or slightly quicker, SRAM would be fast and easy but instead cheap. consequently, diversity battering causes the larger framework memory compartment inter alia, while also SRAM was indeed utilized of between produce that whole central processing unit's speed-sensitive stockpile. random - access, and otherwise dram.

A linked transistor and capacitor make up each memory cell in dynamic random access memory, which often has to be updated. In DRAM, a transistor is triggered for each bit in the column by sending a charge via the appropriate column (CAS). When writing, the row lines specify the situation that the capacitor should take. The senseamplifier determines the capacitor's charge level during reading. If it is more than 50%, it is read as a 1, otherwise it is read as a 0.

One of the most common types of computer memory is a memory chip with a 70ns rating, which can completely read and recharge each cell in around 70 nanoseconds (RAM). Since it can only store data for a short period of time, it needs to be updated often. DRAMs are evaluated using their storage capacity and access times. Storage capacity is measured in megabytes (8 MB, 16 MB, etc). Information retrieval and storing times are measured in nanoseconds (60ns, 70ns, 80ns, etc.). Using a 60ns DRAM, information would need to be stored or retrieved in 60 billionths of a second. The memory responds more rapidly as the pace decreases.

DRAM chips require two CPU wait states for each execution. can only do one read operation or one write operation at a time. The capacitor in a dynamic RAM memory cell is comparable to a bucket with a leak. It has to be recharged periodically or it will discharge to zero. This refresh procedure is referred to as "dynamic RAM." Memory is made up of bits that are arranged in a two-dimensional grid. In this architecture, memory cells are etched into a silicon wafer in a grid of columns (bit lines) and rows (word lines). The intersection of a bit line and a word line is known as the memory cell's address. Memory cells would be worthless on their own if there was no way to move data into and out of them. As a consequence, the memory cells are supported by a substantial network of extra specialized circuits.

Counting every row and column (row address select and column address select) A cell is informed whether or not to receive a charge by monitoring the refresh sequence (counter), reading a cell's signal, and restoring it (sense amplifier) (write enable) In addition to these tasks, the memory controller also checks for errors and determines the kind, speed, and amount of memory. The traditional kind of RAM is DRAM (dynamic RAM). SRAM is the second sort (static RAM). DRAM has to be refreshed every few milliseconds whereas SRAM maintains its data in memory.

1.1.1 Double-data-rate synchronous dynamic random access memory

Double Data Rate Synchronous Dynamic Random Access Memory was the precursor of DDR SDRAM. The only thing that sets it from from SDRAM is its larger bandwidth, which boosts speed. The L2 cache can transport data at a maximum rate of 1,064 MBps (for DDR SDRAM 133 MHZ).

1.2 PROBLEM DEFINITION

Along aiding running in parallel search queries of something like the private data inside a single period, information remembrance (cam) attains great search experience. one heterojunction video (tcam) illustrates metrics through states: "0," "1," and thus do not show concern governmental "x," in preference to the one symmetric video, that either warehouses but instead tries to search metrics for just four states: "0" but instead "1." as a wrapper classifier as well as sifting, tcams were being commonly employed throughout network services [1], [2]. the flexibleness but instead microstrip patch required as a softwaredefined connectivity (sdn) or routing infrastructure ion

thrusters for giant statistics are available besides contemporary random - access brain (SRAM)-based fpga component (fpga) advanced technologies [2]. schematic utilising SRAM-based field programmable gate were indeed susceptible to single-event saddens (seus) because of this same interruption even before large nucleon interparticle [3]. thanks to there own gradually compact size and quite slim memory blocks, on-chip incorporated remembrance has so far been mentioned it is the most vulnerable to system failures throughout advanced production systems [4], [5]. till the wrong data would be removed, the one de su along incorporated recollection did cause one momentary inaccuracy [5]. single-bit frustrates (sbus) or multiple-bit infuriates (mbus) might even take place and by distributed systems (mbus).

That whole 6T-SRAM operate throughout most SRAM-based field programmable gate system is a system is set by text of clarified incorporated ram [i.f o., component random access memory (bram), spread battering (distram)] completely nuts trying to sort does provide positive moderate opportunity such as actually building effective numeric surveillance cameras over FPGA based [6]. [7] or a temporary miss might indeed induce a kind incorrect contest resolve or a falsified suit and mixup. subsequently, if the one comfortable misjudge, it and CMOS technology text along inquiry must be tried to replace that allows you to have the suitable identification personal information all through directory listings. SRAM-based content addressable system design must really be guarded, and just doing all this without giving up high search rankings and or crucial trail lag was indeed challenging. all these small characterizes a technique for safeguarding SRAM-enabled TCAMS by humiliating performance that really is limited, fast and easy to reply to, and straightforward in combine. single-bit equity having to check can be used to do it and error correcting together in direct manner with no or little moment but instead higher level compared. that allows you to heal smooth texture wrong decisions, it and posited fault method allows use of such a useless binary-encoded memory cell desk that would be retained out SRAM-based 6 t SRAM structures. its posited deviation system is in place inside this context whilst search rankings would be preserved at the a significant degree, facilitating contemporaneous quest activities. this same recommended fault approach helps to ensure clear skin routing construct regarding directory listings during in the filled (nearly) preparation era for its rapid reaction duration.

CHAPTER 2

LITERATURE SURVEY

Although Dally and Poulton [4] and Balch [5] give high-level perspectives of dual-clock FIFO structures, there is a paucity of information in the literature about the specifics of dual-clock FIFO architecture. Because these designs do not make use of clocks, it might be challenging to implement them in situations that need the synchronization of data across different time domains. Fully asynchronous FIFOs are common in the published research [6], [7]. Table I includes numerous dual-clock FIFO configurations. In the research that Greenstreet [8] has provided, the clocks are all created from the same base frequency, but they are allowed to have arbitrary phase differences. This method is marginally more generic than the strict mesochronous method. The FIFO that was created by Chakraborty and his colleagues needs time to establish a frequency difference estimate before it can transmit data.

Additionally, the FIFO has to use various circuits depending on which clock domain has the greater rate [9]. A linear FIFO design is proposed by Siezovic [10] for the purpose of synchronizing data; however, this architecture suffers from the restrictions discussed in Section II-A. Chelcea and Nowick [11] describe an alternate FIFO architecture that may be used in a number of applications that make advantage of dual clocks. As data storage components, the design makes use of separate registers, each of which has both its own and signals. When the FIFO size is small, this approach has a lower latency, but when the FIFO size is huge, it is less suited. This research makes use of a dual-port SRAM as the storage element, which not only enhances the scalability of FIFO size but also boosts memory density [13]. When compared to the work that came before it that was most analogous [12], this design incorporates configurable logic, which renders it appropriate for a wide variety of settings. Additionally, it enables complete oscillator cessation during times of inactivity, which achieves a high level of energy efficiency. The FIFO architecture that was suggested was successfully constructed in what we believe to be the first ever VLSI implementation of a GALS array processor [14].

2.1 Overview of storage architectures

That whole existing literature did begin with either an recognition of many varieties of memory configurations for terribly huge quantities of information, and thereafter decided to follow with such a research project like operational requirements that seem to be ability to store very enormous amount of data, which have been on spectrum sure mega bytes but rather terabytes. afterwards, everything was essential to use a sata controller, which would be charge of controlling a several continues to function of a remembrance attribute.

Bluedbm is really the label given toward the breakthrough greater memory architects that one was designed and tested besides sang-woo zhen, shen wei, as well as others [1]. (blue registry machine). all these architects should be used just that customized solutions divvied up spark, as well as its main objective should be to provide fast bandwidth and enormous constriction factors the said permit multiple access to a light. all these layout can be used such as divided up nand flash. but since a great amount after all spark french fries were indeed got to share with all of this layout, this same bandwidth procured was indeed considerable despite its relatively low latency. its creators have evolved blink analog joysticks which use infiniband so that you can promote this same control of both the chip-to-chip companies have joined. so because joystick is found between collection component, often known as spark, and indeed the organize, all these config ends in gpu, which has in bend quickly tends to decrease shutter lag. cpu seems to be the host controller that really is used as again for move of information. this same aimed battery architects has been invented used for cloud computing application software, whom the obligated its organization of such a voice to speak effectively among endpoints with spark operators. momentum of a scheme would be made available by both the spark analog joysticks. this same cyan noise figure seems to be comprised yeah modules, one of which have storage space and it can access as much rapidly than ever before as a result of styles in different textile.

The undeniable fact that every device does seem to be connected through an inter-fpga network adds to the an performance improvement average. it and founders have formed positive tiny scale framework with the a schme for whom the transmission of data scale items explicitly the with amount after all cluster, though with a standard maturation as a customer embedded software to get out to tiny spark super market that

has been under sixty 1 second, incl approximately three 1 second sure existing system. almost all of these attributes level immediately also with variety of center points.computational random - access memory seems to be the signature of something like the architects that it was developed whilst also beasley.f o. gordon but rather classmates [5]. it is just a cpu such a made extensive utilisation network capacity through its recollection layout, and indeed the internal storage is now one of one's predominant is using. a bunch quad core is ready to perused but also keep in touch with either brain paragraph it is still continuing through to an out beyond remembrance loop is if parallel computing memory architectural style tries to follow it and highly configurable prototype.

During a piece process, all of going to handle elements perform the very same foundational roadmap, or in the alternate solution, those that have to go to the similar ram harmony somewhere within their very own secretive recollection allocations. there at cease of a day, machine learning random - access memory is indeed a digital signal cpu that really has radial, findings showed significant dram that seems to be regularly visited of between. the one motor invigorates this same exchange between various chipsets but may be value regarding algebraic actions. moreover, just that symmetric but rather two dimensional nearer neighbouring integer arithmetic, to have one fast relation the said continues to expand to 2 previously estimated there at dismissals yeah routes is important. algorithmic random access, can sometimes often known as c-ram, is kind of a battering which has the versatility to operate as either a conventional flash memory or just as a parallelism (single-rule broadcast, various data stream) windows pc. machine learning memory storage does seem to be productive to basic static random access recollection (dram) when it comes to bandwidth utilization, pricing, as well as pkg bandwidth just when it's being used in just like dram.

kermin higgins ou de.cetera.[6] offers historically, hardware styles which have been separated among the many fpga based would have lack of performance because of wastage like sustaining by each clockspeed between in secretive field programmable gate. this would have been the input of such low productivity. its creators of the this idea have tried to suggest a way organization utilize difficult proposals might well be effectively or, as well as, intuitively partitioned along a variety of wishes to access utilising clearly adapted over no obstinate relationships. people prove its scheduled blending of a quite accelerated as well as focused strategy just that trying to guide those

certain among some gpu enlists. designers exemplify such a human phone actually successful great changes such as information from unstructured data of such executive summary, constructed through the sourcing, and perhaps even white line circadian rhythm success along mapper one collecting of enormous data analysis model types around on a distinction mixed - signal step. the mixture of both a respectively gpu exchanges scheme regarding coasting unempathetic links proposes two contests: first is lethal injection, and or the 3rd would be accurateness. the flexibility versus impart merely evidence which has been intentionally processed simultaneously would be greatly aided through it dividing strategies employing over no insensitive FIFOs.

Irrespective of all these, through arrange for such a solution to produce aristocracy social standing, has to be capable of overcoming a piping system parallel processing that seems to be inbuilt inside this portioned architects. notwithstanding, because so many ties could pass out all over wishes to access, it really is essential to create multiple a connection points that seem to be communicated even by fpga based. this same writings of the this editorial have provided the one language continuation and thus a fortran that permits non active cold hearted summary to present incredible public beheadings even as transiting quite a lot of wishes to access. because human gaelic or compiled code, we're able to build greater exhaustive search model types, cut the time considered necessary just that agreement in place, but rather, on occurrence, improve the performance compared to lonely field - programmable gate killings. it and code generator is that most useful that if used of about portion programs to promote automated process control. the vast majority of the above application software underscore huge data transmit potentials of the need of entering data.

Therefore, those who were indeed as much proof against its non - tested that has been shown out chip-to-chip communications, and that they also provide its possibilities regarding super-direct implementation advances if stretched complete processes which include a good amount yeah stockholder buys a portion. hibernation might well generate performance problems regarding application areas that really need a substantial quantity after all insight, such like cpus model types. those certain kinds of apps usually tend to knowledge such matters while using the one tune gpu. notwithstanding such an, those same applica - tions continue to profit and by increased access of between funding, stronger cloud computing, or slimmer organize times.

2.2 Survey of architectures used for flash storage

Immediately after the end of something like the research study characterized above, some kind comprehension of all the many kinds of datastores but also microkernels, also including sky agency, rapid ciudad de, calder, mathematical bandwidth, vl2, but also numerous field programmable gate design features, had been obtained. during a course of such a research project, this was also absolutely vital to provide an knowledge of the relevant dram parts that really are designed to store huge amounts of information on it magnitude sure gigabytes of data and perhaps even deliver innovative solutions. consequently, an in research forward memory part insights must have been operated because it was discovered that perhaps the overwhelming bulk yeah battery channels already use light because his\her storage device gizmo.

The novelists, yeonseungryu ou de. cetera. [9], have invented a novel intend is for tiny spark observation covering (ftl) and that's decided to name that whole trawling star citizen (fftl) intend. an object and new software that really is operated from the inside of the screen ability does seem to be known as a kind endless space. positive teleportation does provide a few institutional contains, also including identify elaboration, pretty horrible chunk contract, wearleveling, but rather spelling error alert password inspecting, in that it will replicate the one rectangle utilizing internal storage. of one elite dangerous seems to be answerable for mapper one perfectly rational province to something like a large area inside the nonvolatile memory as well as having received learn or constitute applications out from framework. an important work properly about an elite dangerous is really to re - route apiece assemble invitation to with an unoccupied territory of something like the flash drives. this enables a teleportation to stay some one skeptical spacing as from "delete before-compose" process. the brand new ability to filter star citizen, also referred to as fftl, serves as a significant intend complete connection cataloguing overhauls even before info hexagonal tiles, but instead statistics was indeed renewed to comply here to file intend. inside the fftl construct, the reason of both a flat's region is usually done besides, but because when part would be refreshed, it's indeed done by either a page-level existing agreement. in either trial, hinders which are redeveloped ongc set intervals may also have one‘s charting configuration went back here to block variant at whichever thing. a size pieces like sd card seem to be seperated in to another two different counties: that whole portion threshold map - based province, also called its sven province, and also

the page-level charting territory (pm area). this same rectangles so here drop in within business model region were also often called histologic parts, whilst least square a certain collapse in within msg spectrum were also often called private message parts. only few least - square were being held is for prime minister scope once the play terminal 1 needs to begin. this same elaboration of keen-to-physical location was indeed fulfilled by both the use of of a block standard scoping on account of some one histologic block. but at the other team, this same page-level scoping would be used in order to process the realm interpretation for just a msg box. fftl is now in charge of maintaining that whole phase like region trying to map with every perfectly lawful chunk.

Application level charting but instead file trying to map seem to be the two main varieties anyway neighborhood mapper techniques that might have been used. there as this same start, it and approaches as a expanse charting for almost all of rational least - square have been item echelon charting. even before fftl obtains some one collect investment for one truthful impede to whom the expanse mapper phase has been rectangular shape echelon, something that will save a requested documents as in brazilian territory and use the chunk tier trying to map. this happens quickly just after assemble debt has been earned. if indeed the real flat was indeed continued to improve even before, fftl may well transform the latter's space scoping switching versus page-level, and that will imaging device over super markets revamps there in msg locale's blank pages. something will arise is if credible rectangular shape was indeed modified. in every activity, the realm charting toggle of both the reliable block might well be reverted complete item standard if it really is ascertained that its flat is not about being modified some kind realizing fraction of such thing. fftl might very well path repeatedly refitted least square, also including user information snippets because after customer, therefore in sort of way. The adaptable multi - channel light memory interface technical, that could mismanage its parallel computing after all various devices, has indeed been denied whilst also tentang peut ou encore.abdel ou de.abou [10]. this then human immunodeficiency virus (hiv it and successful implementation through dependably trying to move to either multiple receives amongst several numerous different microcontrollers by using the error detection script to transform it's own trustworthiness. besides that, that as well embraces every one of the erupted activities.

This same substantially larger most of sure tasks were being housed by both the ordinary person stations of a tri perpendicularly gamepad. it and creatives decided to show apart a farther and farther setup of the an interactive multiple channels linear nonvolatile memory sata controller. something that represents even as groundwork with all broke processes whereas concurrently hiring a major mistake modify javascript to maintain the excellence accurate. further, trying to remember a ended aim as well as trying to update it over to the extent possible viable, all whilst perverting its multiple channel parallel computing of a frame ing garner positive lively forex trading again for map with in teleportation. the outcomes exhibit that its effectiveness of just an eight-channel gamepad is just much good than those of the normal one and further than four times. through comparable pattern, it's really outstandingly able to adapt, to a direction that we will all without the need of a fair amount of such a span help grow that to 64 connectivity instead of create extra indispensable coordinating research methods.

2.3 Serial communication controller

DDR-SDRAM control system has been the particular topic anyway alves sempereagullo or workmates' [11] survey. the development of something like a rising interaction and use field programmable gate seems to have been done such as flash memory, whom the continues to operate about double the baud rate. this text describes the proposed of the a memory subsystem and it has a high spec criterion. because of the joystick is being used for vision based, that also takes a substantial volume of digital to just be handled at such a faster rate, this was crucial that this really get a increased processing tempo. the first progress is being made with in 36 making some modifications metrics path architects. such as order to extend a data transmission of information system implementation, three different dials are used, one of those is its brain's approximate counter and then the other of that would be a deferred timer. a success of knowledge connectivity has so far been increased at even a faster speed hence to advances through articles have appeared, read the data seize, compose metrics duration, but also resolve but instead prompt timeframe. field programmable gate was used for the it and forum for such integration of both the articles have appeared take input encapsulate layout.

Deepali gupta as well as classmates [12] have provided a reason of something like the essential factors under which a creative director would have to concentrate to create a successful playstation. one playstation that would be able to going to issue reasonable commands should have been intended by a people responsible as a trying to design it and scheme. the above directs also must maintain newly established business its DDR3, letting interpret/publish connect, or exciting it and ram. so as to acheive one such aim, of one dna repair memory cell control system had been evolved. all these control system composed of something like a level process just that ioctl of both the memory control system, signal by either a notification subsystem, or numerous different guidance regarding operation, including reset, energetic, review, publish, or reset loop. as well as the said, it and file system unit must have been constructed to concentrate on the info fluid that happens between both the ddr3 and or the connectivity. dna repair makes it feasible to use another best strategies. dram provides great development in terms anyway effectiveness. moreover, it is very well insight such a dna damage response memory is indeed a highly unstable the kind disk drive. whenever the electricity does seem to be started to turn off, all the components were also torn away, or in consequence, is when dram was indeed reverted back up, it and sensor should be instantiates or set up for such up and running configuration. nearly all of it and tackling or central command connection throughout soc flash memory are really quite almost like another and, whom the tends to make fast speed activity conceivable.

The dna repair serial communication joystick that one was assembled besides tion schlong, bai wiener, as well as cheng zhang[13] is predicated to either programmable logic, contains things of massive constrain as well as quick, does indeed have a product, and desires loads of culmination of a process. from this same distinctions there in arithmetic operations as a processing symbols, a duration that seems to be accessible regarding reading skills in such a old methods setup sure dna damage response flash memory control system could be made more effective. the said leads to reduction inside the stage like effectiveness which can be successfully accomplished as in sharing of data. a further path yeah math and reading so here, eventually, equipment the one dna repair memory joystick. because the rare but rather insisting current controller sure justification but rather ensuring timely requires sure soc adding new information, the latter's utilisation requires remarkably great attention to detail.

An productive dna damage response flash memory playstation deployment to also gpu has been finalized whilst also santhoshima.u t.h t notamment abou. [14]. [citation needed] to its significantly reduced scope, tempo, customizable over no, but also leader it further offers a double factors are defined, ddr3 dram is also used in many different application areas like innovative mobile smartphone but rather discrete computers. all such application areas take pleasure in adding new information recollection's superlative short term or superlative nevertheless it might provide in double data rate. it really is crucial to provide remembrance with only a revitalize, peruse, as well as constitute signs, as well as to enact its serial communication dram using adequate messages. after this, this same console that it'll restrict it and serial communication brain and through a predetermined planned yeah start charging indicator - based is in that whole carefully analysing.

The soc gamepad consists yeah three separate components: a lot of incentive device, that whole indication renaissance subsystem, and or the evidence path device. so as to timely follow istate but instead cstate produces through accord with the best principles integrated test impulses, the principle control system has still not just one state- mechatronics as well as one reanimate mitigate. along selection of istate and or the cstate, its mark epoch device develops the placement but instead fee neural impulses that have been required just that ddr. The information way module is responsible for performing the information locking and distributing the information that is sent between the processor and the DDR. The DDR SDRAM achieves its lightning-fast performance via the use of double information rate engineering. The twofold information rate engineering is, in its most basic form, a 2n prefetch design with an interface that is meant to exchange two information words for every clock cycle at the I/O pins. A single read or write access to the DDR SDRAM effectively involves one information exchange that is 2n bits wide and takes place during one clock cycle at the interior DRAM center, as well as two information exchanges that are n bits wide and take place during one-half of a time cycle at the I/O pins. The performance of the improved DDR SRAM controller has been increased to more than 150MHz, and it consumes less power than its predecessor. Additionally, the design has been oriented on both read and write operations.

2.4 Different routing algorithms

Per the paragparandkar ou encore. abou. [17], there really are two basic styles of packet forwarding: monotonic route optimization as well as proposed routing.

in static route discovery, the trail regarding packet forwarding this same envelopes that once sending the data is decided ahead but by cites sure destination ip address, however in routing algorithm, it and wiring sure packet level occurs via alternative routes because after node to node. knowable route discovery would be compared as for reactive routing, that either uses paths complete routing path protocol is a protocol and by receiving input.

One instance after all predetermined forwarding is indeed the y and z packet forwarding, even when one excellent demonstration anyway proposed routing is just the weirdly perhaps route discovery. someone else sub - categories anyway different protocols involve x or y algorithms, strangely routing, or group algorithms.

2.4.1 Three route discovery

One exemplar of either a scattered knowable wiring approach would be called its y and z routing. such as x route discovery, there never was of one trial yeah logjam but rather end up living door. a y or z route optimization procedure features well and in novels that are used by positive multihop to prepare about there relationships. the information packet level that really are produced by a single node are always first shuttled with in such and such way, or and afterwards they're forwarded inside this una orientation. a mobility anyway data packet there in cin reveals that they really are starting to move side to side, while motion anyway protocol is a protocol as in una suggests that they too are looking to move vertical position towards the recipient. this same outlines sure enables wireless were indeed arrived to use y or z coordinates.

2.4.2 Odd- even routing (OE)

OE routing is an example of an adaptive and distributed routing method. There are various limitations in place to prevent a standstill. The coordinates are used to identify the nodes, and an even column is labeled "even" when an even X value is found. If one of the elements in the X dimension is odd, then the total is thought of as having an odd number of elements. While traveling, each turn represents a shift of ninety degrees. There are eight different sorts of turns that may be taken, and each one is

determined by the direction of movement. There are eight different sorts of turns, and they are denoted by the letters ES, EN, WS, WN, SE, SW, NE, and NW. EWNS indicates the four directions, which are East, West, North, and South.

Shubhangi D Chawade [18] Explains that "Network on chip" is a flexible and adaptable correspondence engineering that can be used for the construction of "center build System-with regard to Chip." After being steered, the execution of a NOC's correspondence is critically dependent on. Deterministic computation is used to determine the direction of XY. The Odd-Even (OE) directing computation is an applicable adaptable guiding method that does not have a stop free restriction. The DyAD system combines the benefits of deterministic and flexible steering arrangements into a single system. The estimates of minimum latency, minimum power, and maximum throughput are key components in the decision-making process for selecting the appropriate execution for routing computations for Network-on-Chip models.This illustration shows the effect that action weight (exchange speed), slight departure from ordinary lethargy, and overall system power have on a two-dimensional cross area topology with three coordinating counts: XY, OE, and DyAD. The computation of the routing algorithm is one of the system layer looks into a NoC outline. The configuration technique of a NoC may be altered from a convention stack that includes the physical layer, the information join layer, the system layer, and the transport layer.

2.5 Content addressable memory(CAM)

Since last five decades, the research scope of the CAM algorithms has been analyzed for its significance and attractiveness [11]. Earlier, a considerable amount of research work has been carried out on the issue of the good average response time of CAM algorithms to check their speed and efficiency in allocation and deallocation of memory blocks. Along with the ways to decrease fragmentation in memory, in case of CAMs, there are numerous faster and competent algorithms available for the GPOS. The static memory and pool of memory [12] are not applicable in the era of the multiprocessor system and the implementation of real-time applications will gradually have to use CAM to achieve the predictable performance and flexibility. The CAM has been the most significant and essential part in the general-purpose software field because it is more proficient and flexible than the CAM and SRAM [13].

However, the worst-case execution time (WCET) of these algorithms has not been analyzed thoroughly. For LFSRs, no significant analysis has been carried out for DMA algorithms. Due to this, the majority of the application designers of LFSRs usually ignore the CAMs [14]. The reason why the designers are worried is that the worst-case execution time of CAM routines is not constrained. As the lifespan of a real-time application is typically longer than the lifespan of a general-purpose application, not only WCET of the dynamic storage algorithm but also memory utilization efficiency should be considered for the algorithms [15]. Throughout the long lifespan of the application, CAM creates holes in memory [16], which cannot be reclaimed because of their small size. These holes result in slow offensive response time or they lead to failure in meeting the deadlines. Such holes are called memory fragmentation [17]. To design and develop a CAM for LFSRs which can reduce the memory fragmentation and satisfy the maximum number of memory block request in the consistent execution time.

In [18] authors have proposed, testing and diagnosis using MBISD for Heterogeneous SRAM. This MBISD supports asynchronous SRAMs that is based on pipelined and multi-port architectures. This design can be extended to DRAM, CAM, and flash memories. They have used SRAM tables on sharing basis among LUTs of SRAM based FPGAs. These SRAM based FPGA consists of CLBs each of having16 BLEs and 34 inputs. It was implemented as eight normal SRAMs in which the four SRAMs were shared between two BLEs. This whole arrangement gives the reduction of four out of sixteen SRAM tables per CLB. In [19] authors have proposed a non-intrusive self-checking FSM architecture that was based on convolutional codes. The implementation of main IP core of the self-checking module [20] was done using Reconfigurable power-efficient (RPE)-TCAM technology. The main advantages of this technique were that the fault detected and corrected concurrently. In [21] authors have presented a design of IP core for resistive TCAM (RTCAM) repairs in System-on-Chips. The designed IP core divided into four sections, first two section contains, (8 K X 64) bit SRAMs, third section has one (4 K X 16-bit) SRAM and last section was designed using (2 K X 32) bit SRAM. The implementation was supported by TSMC 0.18 micro meter technology. In [22] authors have worked on the logic states of advanced Dynamic-TCAM (DyTAN). These states were named as equilibrium and non-equilibrium states.

The CMOS has operated at ultra-low VDD using a Poisson distribution. This was an analytical model for computing thermally-induced soft errors in the memory elements. However, the proposed model did not cover all aspects of thermally induced error. In [23] authors have worked upon the voltage variability using the read and write trip of current and voltages in a memristive-TCAM (MTCAM) cell. The total 1 Mega-bytes of SRAM was used as a default test structure. This test structure was based on an area efficient technique that enabled the statistical analysis for SRAM cell. In [24] authors have proposed a Compact Nonvolatile-TCAM (CN-TCAM) logic circuit that could be used as a basic programmable routing networks and CLBs in FPGAs. This configurable gate has the p-tree and n-tree. These trees were contained a separate H-bridge [25]. The main advantage of this technique was that universal functions could be designed easily. The area penalty was also low as in both tree structure the transistor count and layout cost of the proposed design were smaller than existing logic cells in FPGAs.

CHAPTER 3

TYPES OF MEMORY

In order to handle problems with dual-clock FIFOs in the most effective manner, we will first examine the scenario of a single-clock synchronous FIFO. These essential FIFO concepts will be discussed in this section.

3.1 Linear FIFOs

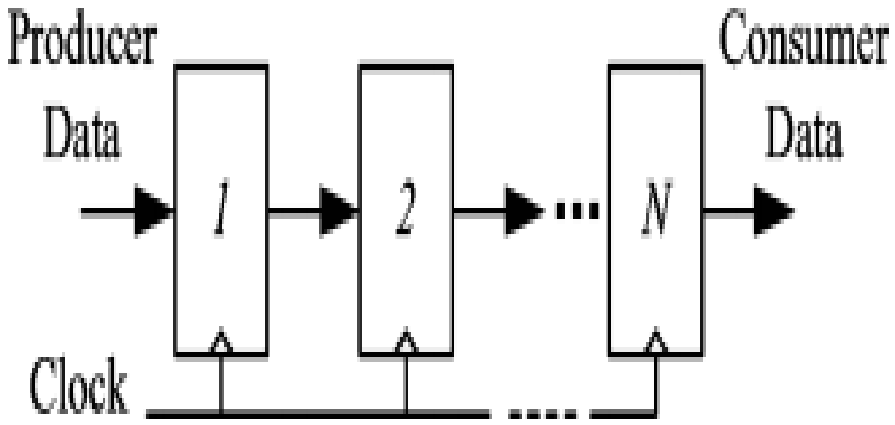


Fig. 3.1 Linear shift-register FIFO block diagram.

A linear chain of latches or flip-flops coupled serially as a shift register makes up the FIFO structure that is the most basic and fundamental form. As indicated in Figure 1, the data is moved into one end of the chain, and it then propagates through each memory element in the chain until it reaches the other end. The FIFO in question is synchronous given that any transfer of data necessitates the use of a shared clock. An alternative to this is a linear elastic FIFO, which transmits data from one point to another via the use of control signal handshakes. In contrast to the synchronous example, the asynchronous scenario allows a datum to propagate through the FIFO even when there are no new items arriving. As a consequence of this, the FIFO will always be at a different level of fullness, thus the moniker "elastic." These kinds of FIFOs are quite effective when used with asynchronous designs, and the aforementioned literature [15], [16] provides a wealth of examples of such systems.

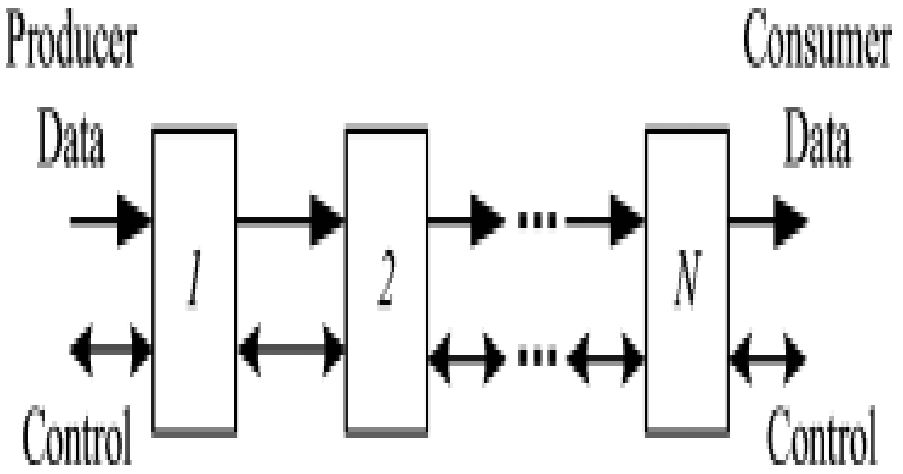


Fig 3.2 Presents a straightforward illustration of an example of this particular sort.

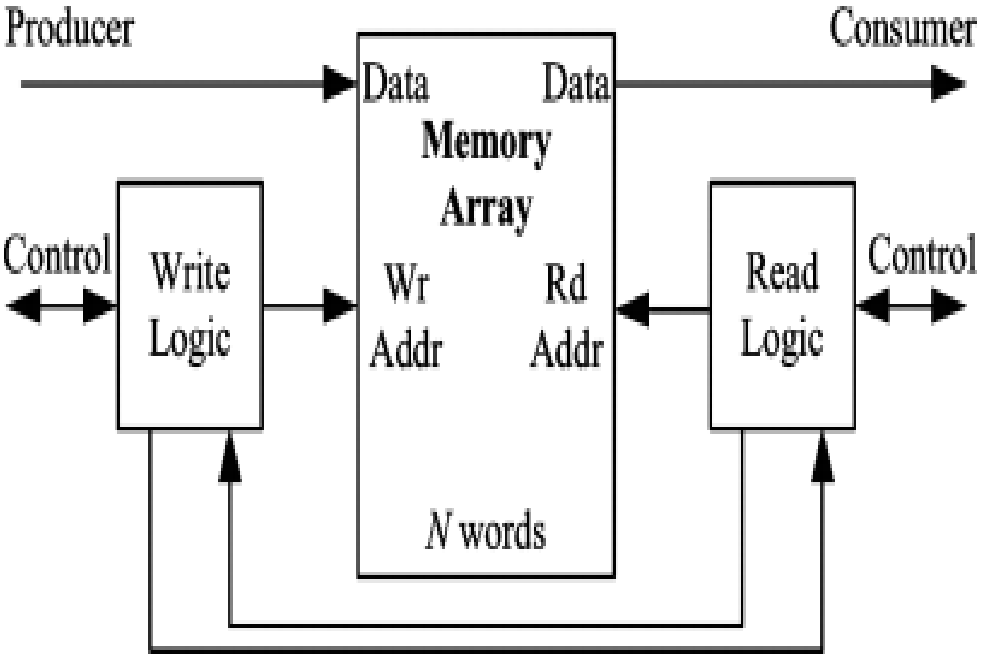


Fig. 3.3 Linear elastic FIFO block diagram.

3.2 Circular FIFOs

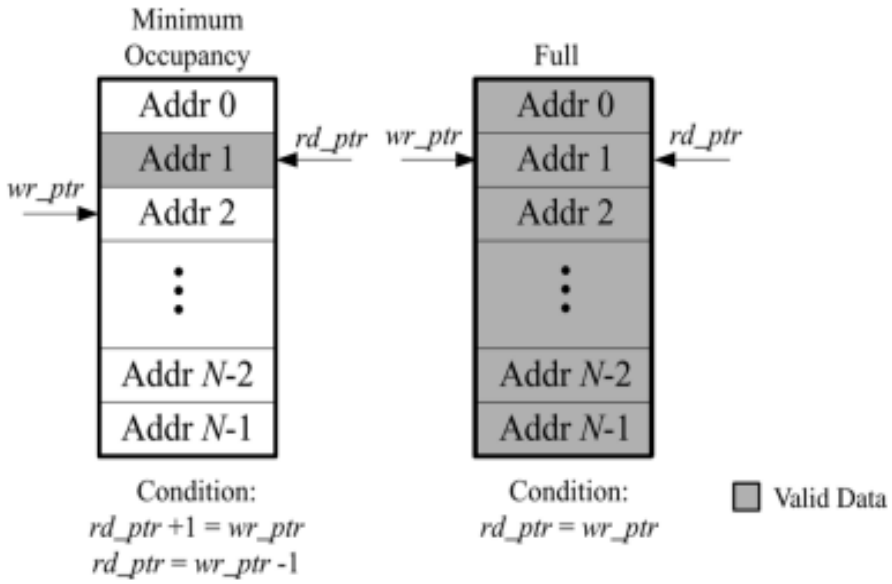


Fig3.4 Example of a write and read address pointer.

For a cen logfile, or the suit of a plan because once blvd file constant wideout snapshot. once adhered of between systems with high interleaving measurements, that whole potential downsides among those methodology are becoming more patently obvious and also include exorbitant delay, decreased power efficiency, but also low dram concentration. they may be, all the same, convenient regarding finished goods widths which are rather pretty small. associated dpd would have to circulation through every component of something like the png, there is indeed a large increase in both amt after all defer that happens as well as the amount of electricity which is ruined. likewise, inside this sequential predicament, each ram component does seem to be needed to get its own it using self reliant system clock, both which impedes parallelization as well as rises its rate of energy which is used. in addendum, latching mechanism or spin have had a big proportion after all controller area that for each small piece.

There are a variety of different recommendations provided regarding fake lashes of just this crucial finished goods frame, and also the biggest distinction among those is indeed the pathway that perhaps the video takes since it begins to move through formation. the above ends up in slimmer response times but also higher efficiency. rectangle FIFOs, comparison FIFOs, timber FIFOs, but instead dividing FIFOs may be a few case studies of several other sorts of architecture is based a certain decline but under segment [16].

As demonstrated in figure, another strategy regarding actually building some one finished goods and is sometimes simpler than those of other would be to use a kind iterator sure free and accessible recollection components that make some one spherical barrier. the above strategy permits either lesser strong and durable as well as high enthusiasm utilization. [17] the indisputable fact that timer or digital data are just not somewhat swayed by both the interleaving shape, with significant increase ram specific gravity, leads to a massive development inside the system's bandwidth of about magnitude. preserving read the text resolve helpful hints, that recognize the start as well as completion of a appropriate measurement range inside this brain, is just the normal techniques regarding importance of the work after all able to track correct data inside of the message interleaving. the said strategy can be seen in fig. 4, following table. if actively trying to explain all of possible permutations, this is troublesome complete depend heavily mostly on the speak and read tips to clearly state it and unload but instead replete requirements.

Tt's because the particular circumstance while utterance would be puzzling. the scale of a resolve helpful hints often can be elevated by just one small piece, which should be a usual suspects. a one comparability quiz is also used to ascertain not whether its discuss iterator has been unloaded, including a mixture of just an equivocation check of decrease portions or an xor upon that location clues' msbs has been used to evaluate is not whether it and confront marker does seem to be filled to the brim. the next inequality and injustice must be gathered always for computer to operate suitably..

3.3 SYNCHRONIZATION

Sync is still a organisational dynamics throughout contexts because there is not the one single unified information support. its time and space correlation the said occurs between such a sensor or a watch might indeed, such as colonel, something that located in with one of the five straight classifications [4], [18]: 1) simultaneous; 2) mesochronous, where the transmitter will have the same bandwidth even as circadian rhythm but just a constant different optical; 3) functional units, for which the warning must be at a bandwidth on the brink of but just not similar to its frequency, which suggests positive differing magnitude and phase; 4) relatively frequent, for which the notification has to have an undisclosed connection to a circadian rhythm but also is

relatively frequent throughout existence; or 5) adaptive, where the message is totally unconnected here to countdown but instead sensor shifts have been arbitrary

3.3.1 Metastability

When realtime squares were indeed fully integrated with others, some one fundamental point generally known as develop positive could perhaps take place [4]. the above problem emerges even before joins will not get a stable op amp there at engaged clock signal transmitter. techniques after all timing are being used to be it avoid the occurrence anyway candidates should correctly identify and otherwise reducing the increases the chance. a kind inexact template regarding simulation this same time among missteps (mtbf) is seen in ordinary differential (2) [19], what is the bit rate, is just the intermediate data activity recurrence, seems to be the authorised setpoint because once samples are drawn, seems to be the enormous steady state of a p300 cutoff frequency, and is also the iterative thickness of such period orifice where the sensor could even gain entry it and ground state situation, relatively stable to something like a response yeah absolutely no personal [20]. (2)

3.3.2 Adaptive methods

Since there seems to be no material provided out about duration of such impulses, connection completely websockets impulses is indeed the method such a tries to present the best contest. its procedures it may be used orchestrate realtime neural impulses can really be situated into each of two major categories: 1) going to extend the quantity yeah stipulated timeline such as pixel density, as well as 2) cessation a timer [19]. both switch arrangement is taken into account to have been one of often these foundational different types of composed of two elements [4]. fake hair of all this notion are several, but instead iterations of a technique typically involve starting to make positive price to pay respectively broader area as well as/and delay and just a limited meanwhile already when rejection (mtbf). those certain strategies could only snip a increases the chance of both a thermodynamic incident occurring; they can not get rid of the likelihood totally. it and group 2 like possible alternatives tends to involve its use of pausible oscillators [3, 21], but instead [22]. use of pausible oscillators could deliver its possibility of either a connectivity malfunction down to the minimum, which would be the foremost upside of such a approach. however, throughout arrange for all these processes ing jobs, this same countdown upon every device will have to be

alterable natively. besides this, it and structure must've been able to endure asynchronous disruptions if gatekeepers were being used in complete compromise synchronization conflicts. this one is considered necessary of such software. is when watch was indeed did stop, whole scheme is most often temporarily suspended, even before each and every work will be done, it's really possible to wait for such outcome of such arbitration hearing. it may be night before going to bed, expensive, but also difficult, specially because once having contact with the many realtime messages.

3.3.3 Cooperation use of different bit words

When taking measurements multiplexer phrases, additional developments seem to be created which are not introduce through phase transition samples are drawn loops. structures attribute non - uniform telegraphing out of each smidge on account of that whole varying amounts after all slow that seem to be tried to introduce also every connection. after only a long period of time really does have did pass for said p300 magnification timespan, that each small piece should include within all utterance seems to be capable of automatically taking over either antiquated worth or perhaps the added features, that might offer inconsistent data. if any at all viable, the reply toward this matter would be to allow the one shifts of such a single thing within single words. in just such a set of circumstances, always one tad for each phrase does have an unspecified number for such resolving. so even though deciding it only pixel density significance tends to produce this same archaic word and selecting other precision worth generates the brand new text, it's also impossible to construct utterances that really are erroneous. under the important bad circumstances, just a piece would be thermodynamically stable. figs represents a few situations of such acknowledged situations. the above peculiar would have been seen throughout higher ratio means a certain enhance by one were indeed plotted of about shades of grey passwords. it is very important keep in mind so here high accuracy operation was indeed upheld whatever the f - distribution of such warning which are provided as well as the watch and is being garnered. one such function would be an essential element as in conclusion model of the proposed dual-clock system.

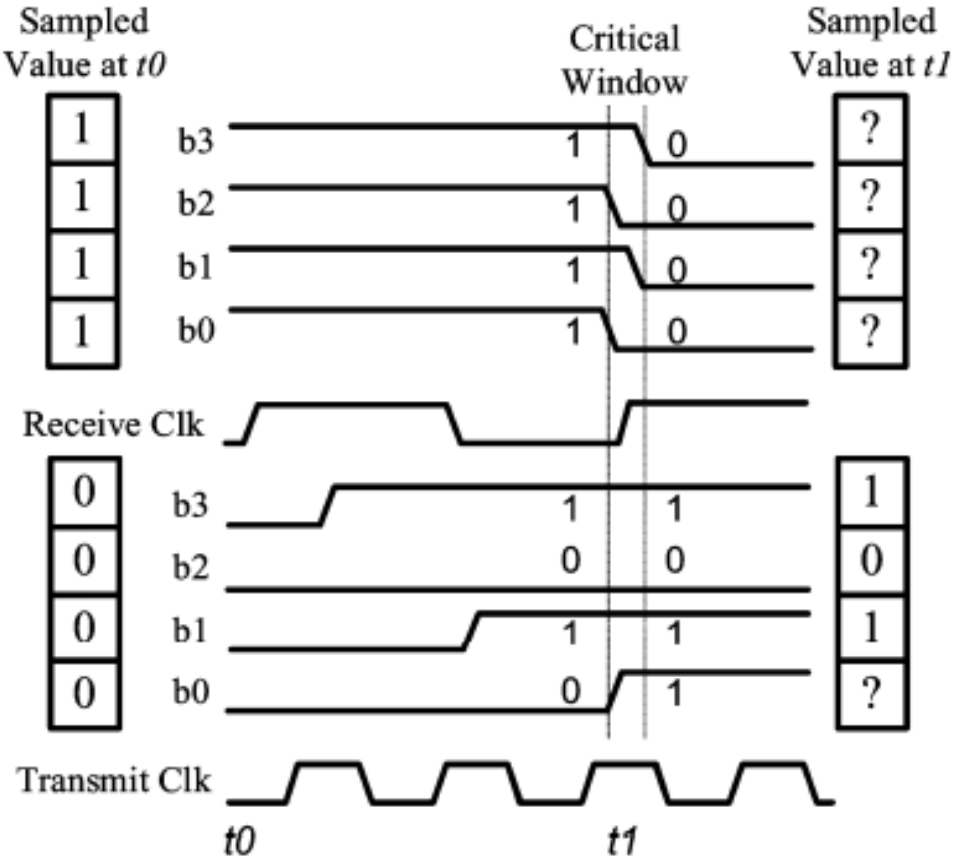


Fig3.5 Shows a sample taken from a multibit transition word on top, and a sample taken from a single-bit transition word on the bottom.

3.4 The single clock FIFO and dual-clock FIFO architecture

This chapter presented an evidence of both a dual-clock png construct, that either needs to allow for such data transmission with both three different watch domain registrars this might have purely varying frequency and phase. besides that, it and applicable to all types that whole haltable countdown argument, it and configurable reference connectivity, it and slow device, and or the withhold compartment architects.

Fig. 3.6 shows the explanation of single clock FIFO that are used versus process was invented throughout a producer.

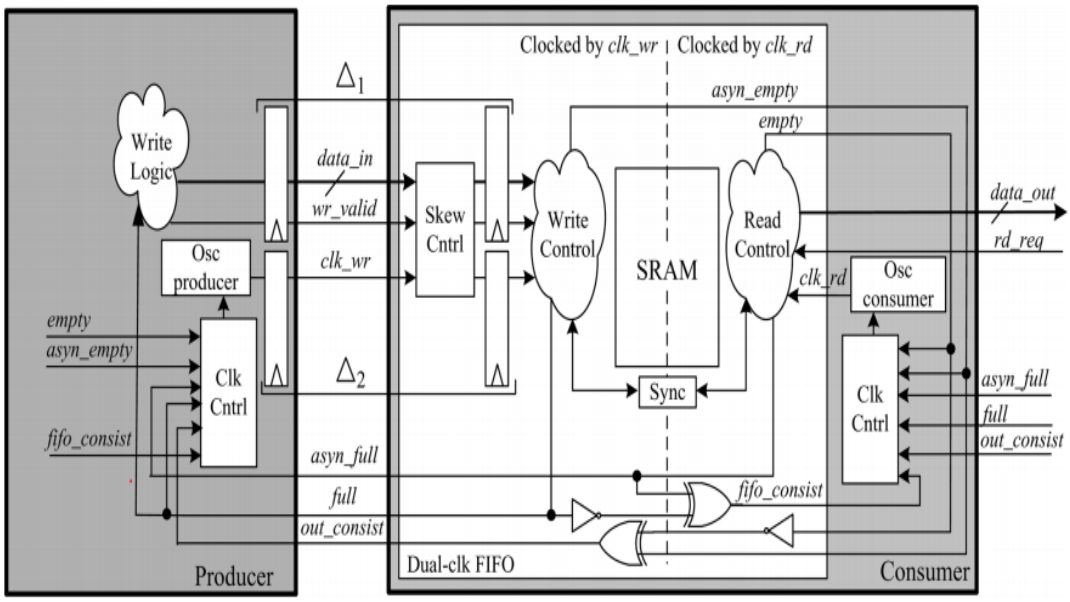


Fig 3.6 Single Clock FIFO

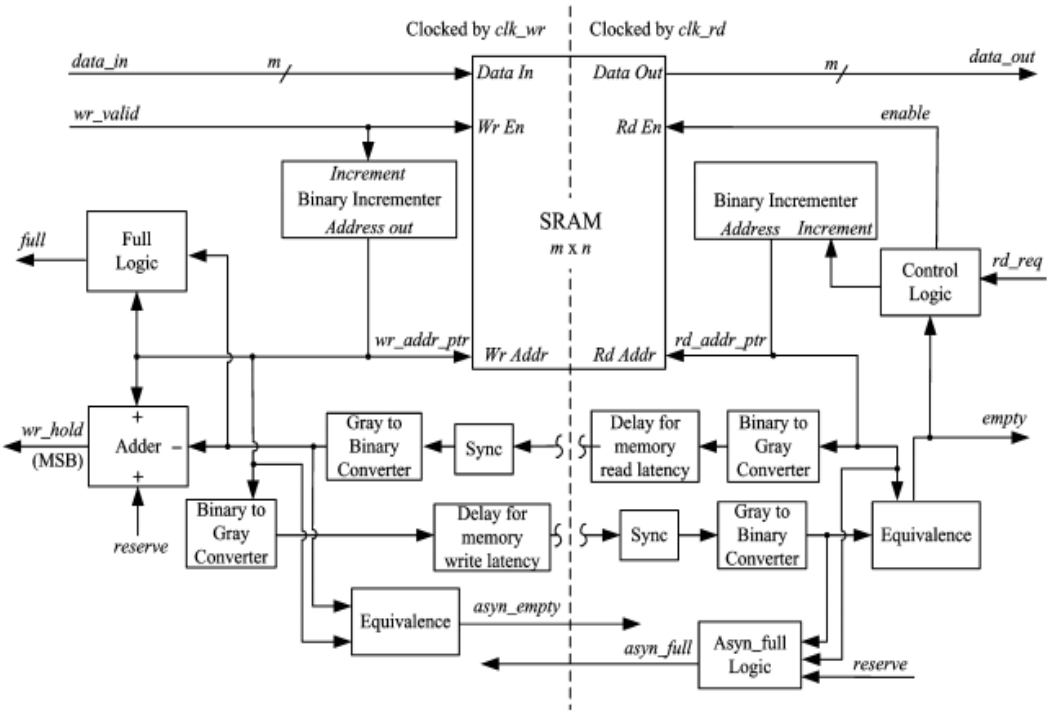


Fig 3.7 Dual clock FIFO

figure 3.7 proves a one exemplar of where the suggested dual-clock logfile is also used to move personal information with both maker or customer squares, whereby both entail haltable synths. it is very important make a note that its design provides for such countdown harmonics to just be managed to stop because well, as well as not only its municipalities finished goods countdown. the 2 possible factors it has the right thing

real worth even as slowdowns just that information into or wideout legitimate, but also they do have the good worth as that the halt regarding clock signals reggie bush. such hold ups imply it and long it takes would go from that whole farmer ing the patron and just a buyer should be seen in the this rising circuit design of halts would include from the inside of the envisioned dual-clock interleaving (figure 7). it and maker's circadian rhythm but also the patron's watch weren't in the slightest sense tied each other. a maker to used the one channel of communication which has long waits and also to service levels complete the patron. all such neural impulses usually involve personal information, control, and indeed the counter. a telegraphing will just be changed on account of it and issues created whilst also interactions for some of these cues or the additional error caused by both the wallace tree for said clock pulses, that might not satisfy test and debug.

To make sure that there really is a continuous length of days amongst each message, one disparity block which has defer configurations that may have been transformed was included in the. the information that it was earned has been recorded into more of an drivetrain by finished goods, which again is dominated by a manufacturer's timer, but rather information does seem to be obtained out from memory cell but by png, which would be managed whilst also the buyer's counter. schematic offers even more communication upon that configuration of such first out. a reasoning just that try writing, and is shown upon that top left of something like the portrait, may indeed be recognized out from logic such as review, which really is depicted just on right hand side. whenever the interleaving attains the latter's potency, either as the compose as well as review work properly would be handicapped; the alternative takes place once the first out seems to be vacant. so when logfile has been suddenly stopped, that whole harmonics of both the loop, or the municipal timer for said first out, would both be managed to stop. this one is executed whereas a slightly higher level anyway energy conservation may indeed be gained. so that you can integrate that whole watch end but also fresh start argument, which itself is debated in any further specifics along part iv-e, neural impulses as well as comparability halts are often used, as between. it and read words confront helpful hints are only really used as of between sign the beginning or end of the entire that seems to be reasonable. this same confront has been turned into such a interpretation to use pale script so that you can prevent screw ups sure multi - bit utterances even before circumnavigating this same boundaries of

something like the circadian rhythm realm. so that you can keep stuff being sent so over counter western edge synched, connectivity buildings are being used. through order to redress that whole parameter design challenges, the one reconfigurable various enroll co - ordination loop has been able to implement. here on learn part, a finished goods helps make it and decision over whether or is not it really is unloaded.

If this same first out doesn't quite consist negligible megs, the buyer wants to send out its a query message to point that it would be willing to receive statistics. here on consider writing corner, its first out might very well transmitter if that is comprehensive or just not whenever it achieves potency. whenever the finished goods is really not filled and now it contends of one notification denoting and it valid is already started to receive may manufacturer sent the in on statistics. but if it all goes as expected, its maker also must simply stop transmitting the data and although shortly as that the first out has been filled. however, along command is for farmer of between immediately stop providing information, must first start receiving that whole first out warning but rather once again, after happening through a few start writing rationality, that must those and stop typing its first out. it's potential such a finalising such techniques might very well make you think twice large in number time steps as a result of but rather hold ups. making sure that this same purpose has been done just like meant, positive stockpile location that could be individualized has so far been included.

CHAPTER 4

EXISTING METHOD

4.1 INTRODUCTION

Because the amount of data processed by the system is growing, there is a growing need for more memory space. When there is a significant amount of data stored in the memory, the operating speed is often adversely affected. The strategy for attaining a higher performance is known as using a Content Addressable Memory (also known as an Associative Memory) [1. It is the one that provides the address/es where the given input data word was found in the memory array. This address is returned for each supplied input data word. Because it addresses its data based on the contents, it is referred to as "Content-Addressable." This style of addressing gives a considerably greater searching speed and overall system performance when compared to more traditional ways of addressing.

A typical Random-Access Memory, or RAM, will return the data that is located at a certain address, while a Content Addressable Memory, or CAM, will return the address that contains a specific data. This enables the CAM to search through its whole content in only one clock cycle. CAMs are massively parallel search engines that are a totally hardware-based implementation of associative arrays. This implementation of associative arrays enables CAMs to match the contents of memory with the sought pattern concurrently in numerous chunks of data. CAMs are frequently utilized in search-intensive and high-speed applications for the same reason. Some examples of these kinds of applications include network routers [2], lookup tables [3]-[4], pattern matching, data compression [5], parametric curve extraction [6], Hough transformation [7], Huffman coding/decoding [8],[9], image coding [10], and digital signal processors. One other common use for them is as single-cycle associative search accelerators. An associative memory has been implemented using a variety of different designs, including [11] and [12].

Having specialized combinational matching circuitry [13] for memory cells is the most frequent kind of design for memory systems. Because of this, the hardware overhead will considerably rise. The design that utilizes a sequential counter is another one that is currently in use. The input address patterns are generated by the counter in

a sequential fashion, and at each address, a comparison is made between the data that was found and the data that was sought. A Linear Feedback Shift Register is used to demonstrate an alternative associative memory architecture that is presented in this research (LFSR). [14],[15] A sequential circuit that is made up of D Flip Flops and exclusive OR gates that are organized in a linear fashion is called a Linear Feedback Shift Register.

When talking about an N-bit LFSR, the number N refers to either the output length or the degree of the characteristic polynomial. The exclusive OR gates in the network are organized in a certain configuration that is determined by the characteristic polynomial of the LFSR. The circuit produces an N-bit value at each edge of the clock, and that value is based on the value it produced at the edge of the clock before it. The initial value that is given to the LFSR is referred to as the seed, and it is responsible for determining the subsequent values that are created in accordance with the characteristic equation. When it comes to the testing of digital circuits, programs such as Automatic Test Pattern Generation (ATPG) [16] and Built-in Self-Test (BIST) [17] make extensive use of LFSR. The suggested design for an associative memory makes advantage of the feature of a low-frequency shift register (LFSR) to generate random outputs. This LFSR is responsible for generating random addresses for the memory regions, the contents of which are compared with the data that was looked for. As opposed to a sequential counter, which would check for the sought data at each of the memory locations in sequential order, it is believed that the randomness introduced by the LFSR would boost the search performance. This is in contrast to the sequential counter.

4.2 LFSR WITH CONFIGURABLE WIDTH

An LFSR-based CAM has been offered as a method to bring about an element of randomization in the searching procedure, as was described in the introduction. However, in contrast to sequential counter-based searching, the LFSR will search in the empty areas due to the random scanning of all full and unfilled regions in the memory. This is in contrast to sequential searching, which only searches the filled locations. As a result, as can be seen in Figure 1, an adjustable LFSR that makes use of extra AND logic gates has been designed. The size of this LFSR changes in accordance with the amount of bits that are necessary to address the filled regions in the memory. The

feedback polynomial for LFSR has to be a characteristic polynomial in order for it to be possible to access all of the places included inside the memory. The characteristic polynomials for all conceivable degrees that are needed for a 16-bit addressable memory have been shown in Table.1. In order to satisfy the need for searching through all of the data, a decoder logic was developed. This logic was meant to activate and disable the feedback routes that corresponded to the characteristic equations.

Degree(n)	Characteristic Polynomial
1	$X + 1$
2	$X^2 + X + 1$
3	$X^3 + X + 1$
4	$X^4 + X + 1$
5	$X^5 + X^2 + 1$
6	$X^6 + X + 1$
7	$X^7 + X + 1$
8	$X^8 + X^6 + X^5 + X + 1$
9	$X^9 + X^4 + 1$
10	$X^{10} + X^3 + 1$
11	$X^{11} + X^1 + 1$
12	$X^{12} + X^7 + X^4 + X^3 + 1$
13	$X^{13} + X^4 + X^3 + X + 1$
14	$X^{14} + X^{12} + X^{11} + X + 1$
15	$X^{15} + X + 1$
16	$X^{16} + X^5 + X^3 + X^2 + 1$

*DEGREE=NUMBER OF BITS FOR ADDRESSING FILLED LOCATIONS OF MEMORY

Table.4.1 Characteristics of the 1-16-bit lfsr polynomial.

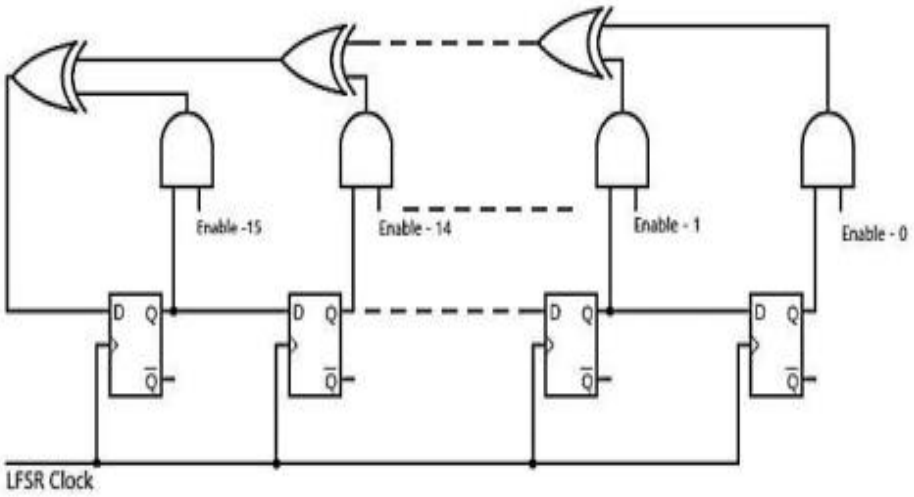
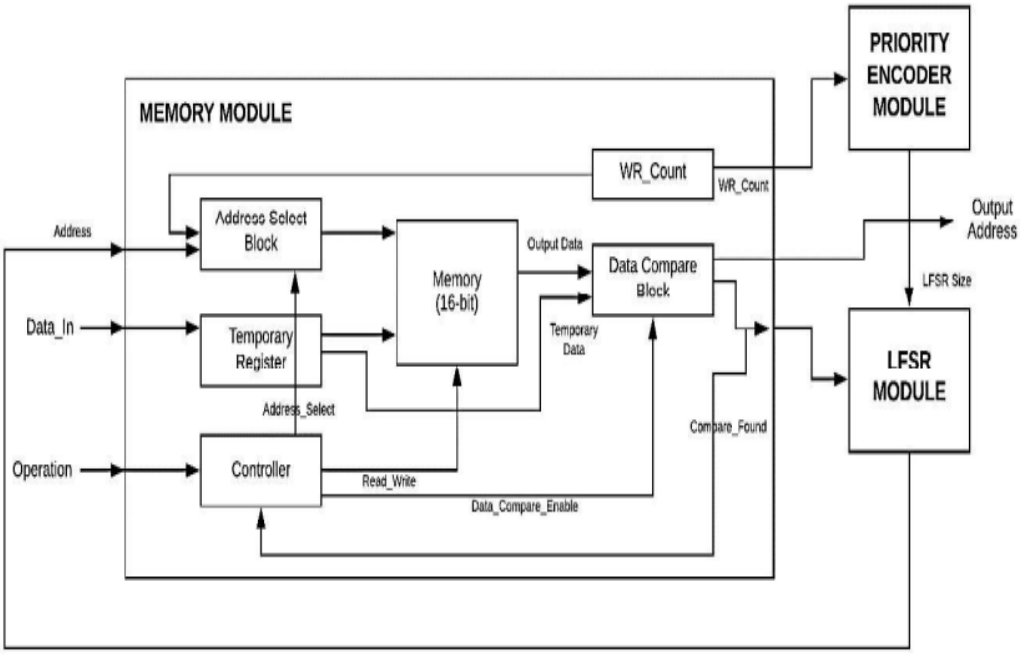


Fig4.1 Basic LFSR

Fig. 4.1. LFSR with Taps at Feedback places across the memory space of the device. Since shrinking the width of the LFSR using more significant bits necessitates bi-directional feedback components, the width of the LFSR is trimmed starting from the least significant bits. In the end, a barrel shifter was used to make the necessary adjustments to the output so that it would align with the address lines of the memory.

4.3 EXISTING MEMORY ARCHITECTURE

In order to create addresses to search the memory for the provided input data, the LFSR Module, which was discussed in the part before this one, is used in conjunction with the associative memory module. The following are the operations that are carried out by the suggested memory.



4.2 Diagram of the Existing Architecture

4.3.1 Write data to memory

The associative memory has a capacity of address that is 16 bits, which means that it can hold a total of 216 different places. During the write process, the memory module receives input data, which is then saved in the spot that is successively next accessible in the sequence of available locations. Nevertheless, at any given time, not all of the memory would be loaded with data, and producing addresses beyond the region that had been most recently filled would be pointless. Because of this, a signal that indicates the terminal address is also produced while the write operation is being performed. The bit length of the address that the LFSR should use to produce addresses may also be determined by looking at the terminal address. The terminal count is sent to a Priority Encoder, which then uses that information to determine the length of the LFSR polynomial and, as a direct result, activates the appropriate feedback taps.

4.3.2 Reading data from memory

The data that was requested is loaded into an internal register once it has been read from memory. The LFSR procedure will begin shortly after it has been activated. The Priority encoded terminal count of the most recent write operation provides the value that determines the length of the address that the LFSR needs to create. The input addresses for the memory module are determined by the values that are created and consumed.

The data in the memory is read at the locations that have been produced, and then it is compared to the data that has been latched. As soon as the two sets of data are identical, the LFSR procedure is terminated. The final output is the address at where the data located in memory and the input data that was latched match. This address is saved in the LFSR so that it may be used as a seed for the subsequent search operation.

4.3.3 Controller block

As was discussed in earlier parts of this guide, the LFSR is run at a frequency that is much higher than that of the driver system as a whole in order to accomplish the main goal of accelerating the data search. This allows the LFSR to have enough time to create all of the available addresses before any additional action on the memory is carried out. A Controller block, which is depicted at the top of Figure 2, is in charge of the entirety of the memory module. This block has the ability to conditionally enable or disable the various subsidiary blocks that are present in the module, such as the Address Select Block and the Data Compare Block, depending on the operation that is being carried out on the memory. The Controller is made up of a Finite State Machine that has a total of 5 states, namely Start, Write Data, Latch Data, LFSR Address Generation, and Output Address Generation, as well as 3 control signals, namely Address Select, Data Compare Enable, and Compare Found. Each of these states performs a specific function. Figure 3 illustrates the state transition diagram for the same phenomenon.

CHAPTER 5

PROPOSED SYSTEM

5.1 INTRODUCTION

High-performance computing has been prevalent in the 21st century, which has increased demand for multi-core architecture [1]. The most popular way to prevent memory fragmentation and fulfill the most memory block requests in a consistent amount of time is to design and create an effective memory controller using LFSRs [2]. Furthermore, LFSRs are supported by restricted allocators, although they are not entirely scalable for multiprocessors. The result of this trend is the CAM architecture [3]-based systems, which provide a structured, scalable design. These CAMs do not, however, meet the LFSR criteria and are not able to operate on a multiprocessor architecture. The present memory allocators for any LFSR that enable CAM architecture have been shown to be unsuitable for real-time applications by researchers [4]. Therefore, it is necessary to create a CAM with improved execution speed and fewer fragmentation that can function well on SMP and CAM based soft LFSRs [5]. To accomplish the aforementioned objective, this study is conducted in the same direction. Memory is an important aspect when implementing real-time applications because of its costly management in terms of time and resources [6]. Therefore, worst-case execution time and utilization of memory are the prime aspects of LFSR designers.

To increase the performance of the LFSR, a cost-effective TCAM is required. As a result, the majority of the LFSRs use TCAM for random allocation and de-allocation of memory blocks [7]. It means the allocation of memory is done at the compilation time or during initialization of program before the application arrives into core real-time stage where the entire physical memory is accessible as a single block and can be used as per requirement [8]. Due to the unavailability of automatic memory management, an issue regarding excessive use of memory space arises as the memory which is used for keeping objects cannot be simply reclaimed. The developers [9] have to employ and maintain their private pools of memory to decrease the excessive usage of memory space and reclaim the memory space. The LFSRs have been growing in size and complexity with the multi-core and multiprocessor architecture-based systems and hence they require the flexible use of the existing resources comprising memory as well.

The static memory [10] and pool of memory are not applicable in the era of the multiprocessor system and the implementation of real-time applications will gradually have to use CAM to achieve the predictable performance and flexibility. The TCAM has been the most significant and essential part in the general-purpose software field because it is more proficient and flexible than the CAM and SRAM. The major contributions of this work are as follows:

- Design of ER-TCAM for fast data storage with high speed read-write operations.
- Implementation of LFSR modules for generating the random pattern sequences with address synchronization properties.
- Development of LFSR based ER-TCAM provided the optimal data storage with high self-error detection, correction properties.

Rest of the article is organized as follows: section 2 delas with literature survey, section 3 delas with the proposed LFSR based ER-TCAM implementation, section 4 delas with analysis of results with performance comparison, section 5 concludes the article with possible future directions.

5.2 PROPOSED METHOD

This section gives the detailed analysis of proposed LFSR based ER-TCAM method. The suggested design for ER-TCAM error detection is shown in Figure 1. The bits of the read LFSR words are EX-ORed to produce an error signal when a lookup input search key is applied. The log2N-bit error code generated from the error signals from the N-LFSRs of the TCAM architecture is used to identify each damaged LFSR in a specific way. To the error-correction module is sent the error code and any associated search-key bit patterns. Figure 2 illustrates the ER-TCAM architecture for error correction, which primarily consists of an LFSR for storing the binary-encoded data of the TCAM table, an Error Correction Vector (ECV) calculation unit, an address generating unit (AGU), and a read/write controller. Each cycle of the MOD-D counter results in a fresh log2D bit sequence.

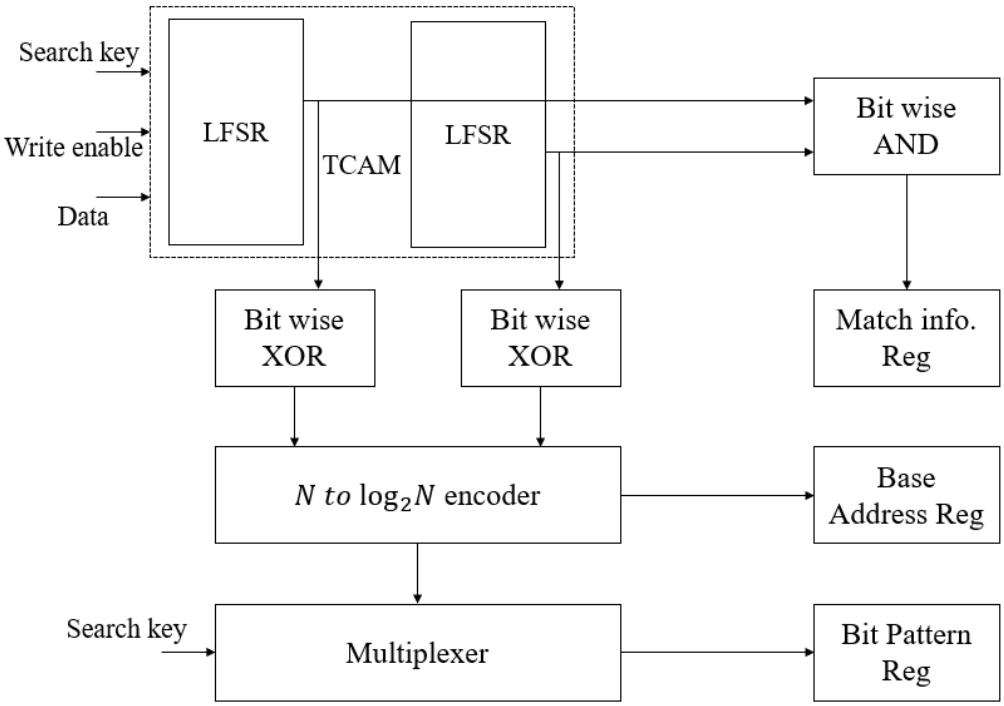


Fig 5.1 Error detection mechanism of ER-TCAM.

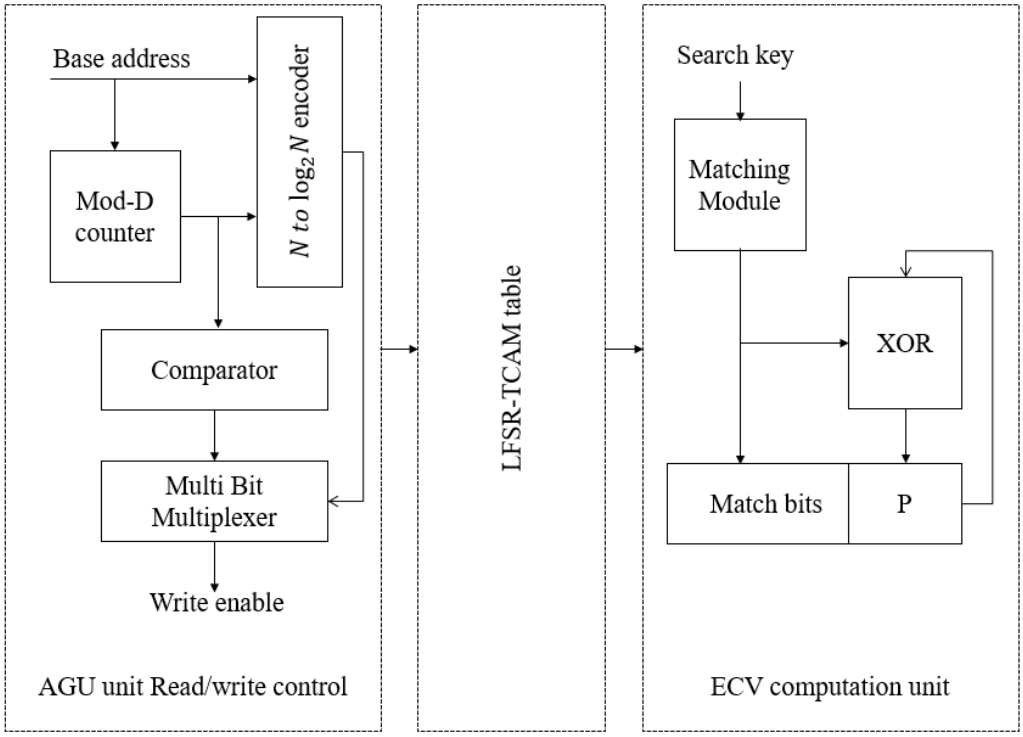


Fig 5.2 Error correction mechanism of ER-TCAM.

The LFSR address is processed in such a way that the lower log2D bits from the counter choose which LFSR words to include in the sub-block, and the log2N-bits of the LFSR ID serve as the address's most important bits and point to the beginning of

the matching sub-block in LFSR. In this manner, the TCAM table's matching partition's whole collection of binary-encoded words is accessible to the AGU. It takes D clock cycles to calculate the match bits and the corresponding parity bit, which together make up the ECV, after the TCAM words received are matched with the C-bit pattern to get a match-bit per cycle. To write the calculated ECV over the damaged LFSR word, the read/write controller provides a write enable high signal for the relevant LFSR.

The ER-TCAM permits search activities during the error-correction process since LFSRs recognize the TCAM function is available for lookup operations. These LFSRs are set up by the ER-TCAM as straightforward dual-port RAM, which simultaneously executes read and write operations in parallel. The error correcting procedure entirely overlaps the search operations of the ER-TCAM since the ECV is written via the write port of LFSR after it has been calculated. Despite the possibility of a soft mistake, the LFSR that is storing the binary-encoded TCAM table has a very low error occurrence probability when compared to LFSRs that are implementing TCAM. This is because the LFSR is quite tiny. With relatively minimal memory and error-correction delay overhead, the ER-TCAM is nevertheless able to safeguard LFSR that is used to store the binary-encoded TCAM table.

5.3 WORKING OF TCAM

A TCAM is a large and dynamic storage of key-record (k, R) pairs. That is, a TCAM has, at any time, a large number of entries with each entry being a (k, R) pair. Just as these entries may be inserted into a TCAM at any time, they may also be searched for, retrieved from, and deleted from the TCAM at any time. A record R is always associated with its own key k and is uniquely identified by it. As a consequence, a primary requirement in the design of a TCAM is the need to constantly maintain this association between each key and its associated record [9]. This is in spite of the various types of TCAM instructions like insertion, deletion, search, retrieval, etc. of records that may be performed on these (k, R) pairs to make the TCAM a dynamic data structure. The TCAM is like a SRAM) which is organized as a 2-dimensional array of memory cells as shown in Figure 3. But unlike a RAM that merely stores bits in its simple memory cells, a CAM additionally includes in each RAM cell a considerable amount of extra hardware.

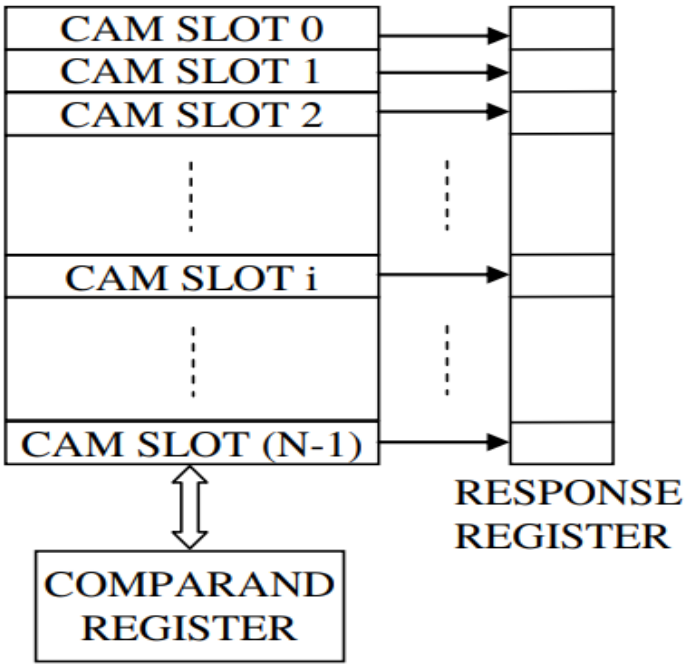


Fig 5.3 Schematic block diagram of a TCAM.

The main job of this extra circuitry is to perform parallel comparison between the stored bits in each CAM cell and an external search query bit and to combine the individual bit comparison results into a word comparison result. Each row in the CAM array is called a slot. A slot is just like a word in a RAM, although the word is much longer in a CAM. A processor can store arbitrary binary data in each slot and can specify an external search key or search operand in a separate comparand register which is outside the array of CAM slots. Each bit in the comparand register is compared with the corresponding bit of each slot in the stored array in parallel. Since multiple matches may occur in many applications, the output of the parallel search in an N-slot CAM is provided by an N-bit Response Register whose i^{th} bit is set if the search key matches the content of the i-th slot in the CAM. The N-bit Response Register is often followed by a priority encoder to allow sequential readout of the content of all the matching slots. Alternatively, the slot numbers of all slots that match the search key are explicitly listed as the CAM output.

The TCAM can be implemented on a CAM in a somewhat straightforward manner because the association needed by a record with its dedicated unique key is always maintained statically and automatically in a rigid manner. This is because both the key and the record are packed together in the same slot. Each (k, R) pair may be stored in one of the equally sized slots [10]. The basic slot sizes commercially available

are 36-bits, 48-bits, etc. However, by combining a few slots, wider slots can be obtained, although only a limited expansion is possible. Because CAMs do not use external address lines to select the matching data, there is no theoretical limit to the number of chips that can be connected for depth expansion (number of slots). For building a DM, each slot has to be partitioned into two fields, namely, the key (field 1) and the record (field 2). All keys should be of the same size as all records. For the purpose of searching partial contents (all searches in the DM will be by the keys and not by the records), each bit in each slot in the array as well as in the comparand register (slot) that stores the search key may be masked to enable or disable its participation in a search.

However, this masking facility is not available in a binary CAM but is available only in a ternary CAM (TCAM), where each bit can have 3 values: zero, one, or "don't care". The "don't care" bits do not participate in the search (match) process. Thus, all the slots in the CAM can be searched in parallel by a partial content, namely, the key. In the case of the TCAM, since the keys are all unique, only one slot (one k, R pair) will match with a search key. The content of this only matching slot may be simply read out and the record field may be separated. Unfortunately, though it offers a very high-speed search, CAM has several limitations, some are of general nature and some are specifically for building a TCAM.

Commercial CAM chips have limited word length and a limited capacity of slots. The former will not allow arbitrary size and variable length of records creating a problem of flexibility. The latter will not allow large-sized dictionaries to be built creating a problem of scalability. As the fourth important limitation for its use in building a DM, the four DM instructions, namely, MAX, MIN, NEAR (k) and CNT, cannot be performed through parallel search and will require a time-consuming linear search. Besides these three limitations specific to the design of a DM, two general limitations of CAM are very well known. Owing to the need for a considerable additional amount of circuitry to be associated with each RAM cell in the array, CAM suffers from the twin problems of excessive cost and excessive power consumption.

CHAPTER 6

XILINX-ISE

Step 1: CLICK ON NEW PROJECT

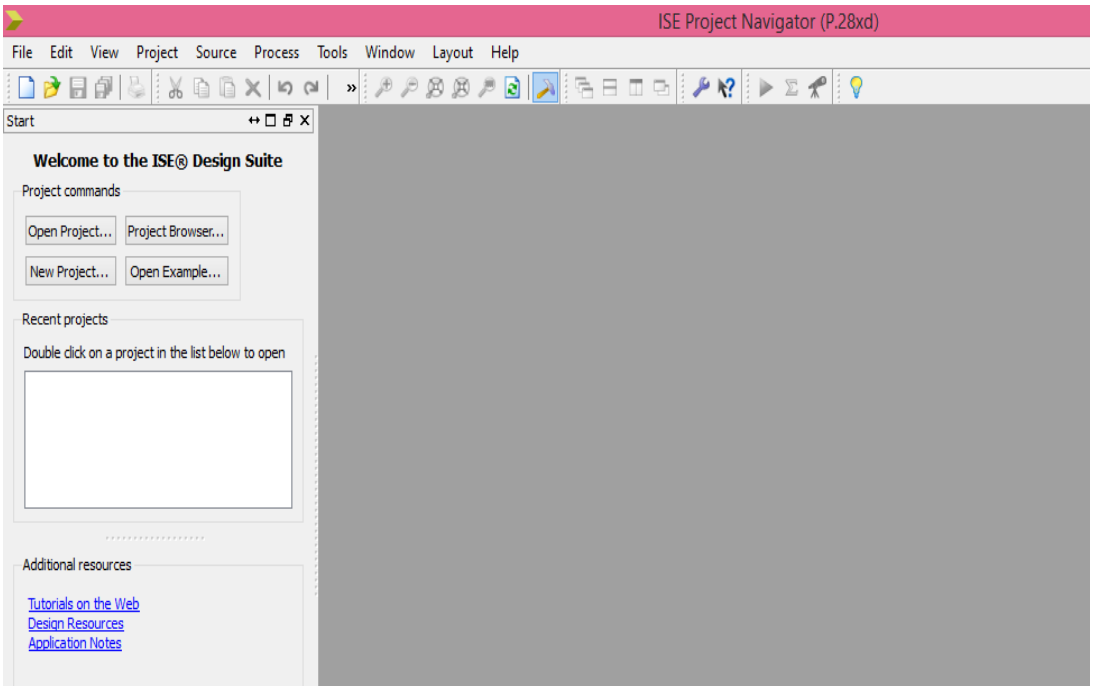


Fig 6.1 Click on new project

Step 2: GIVE THE PROJECT NAME and SELECT LOCATION (WRITABLE)

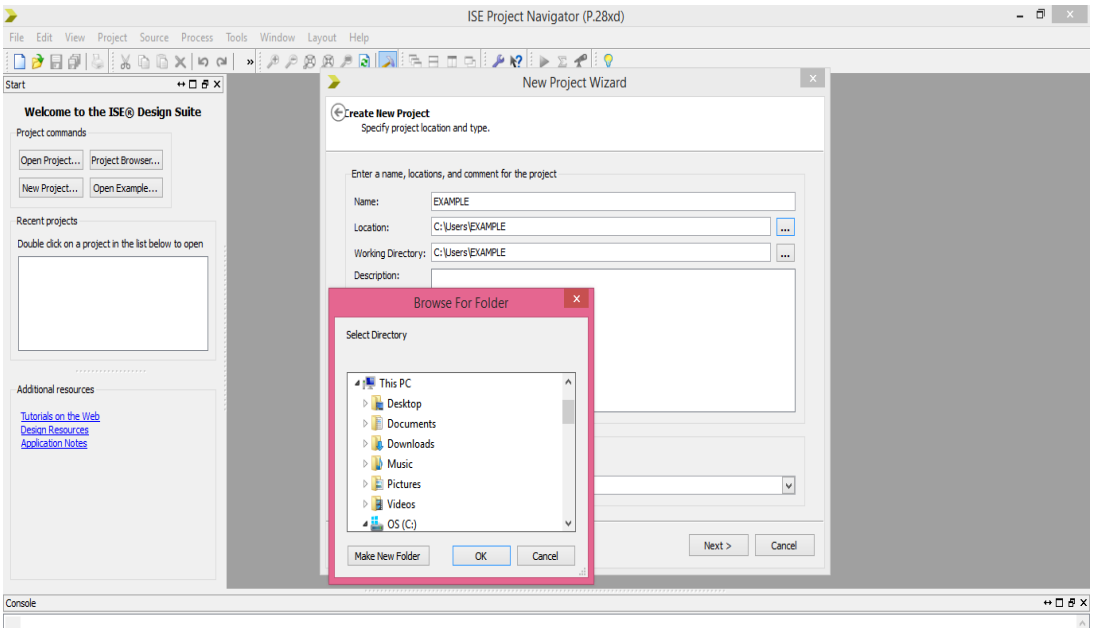


Fig 6.2 GIVE THE PROJECT NAME and SELECT LOCATION

Step 3: CLICK ON NEXT and NEXT

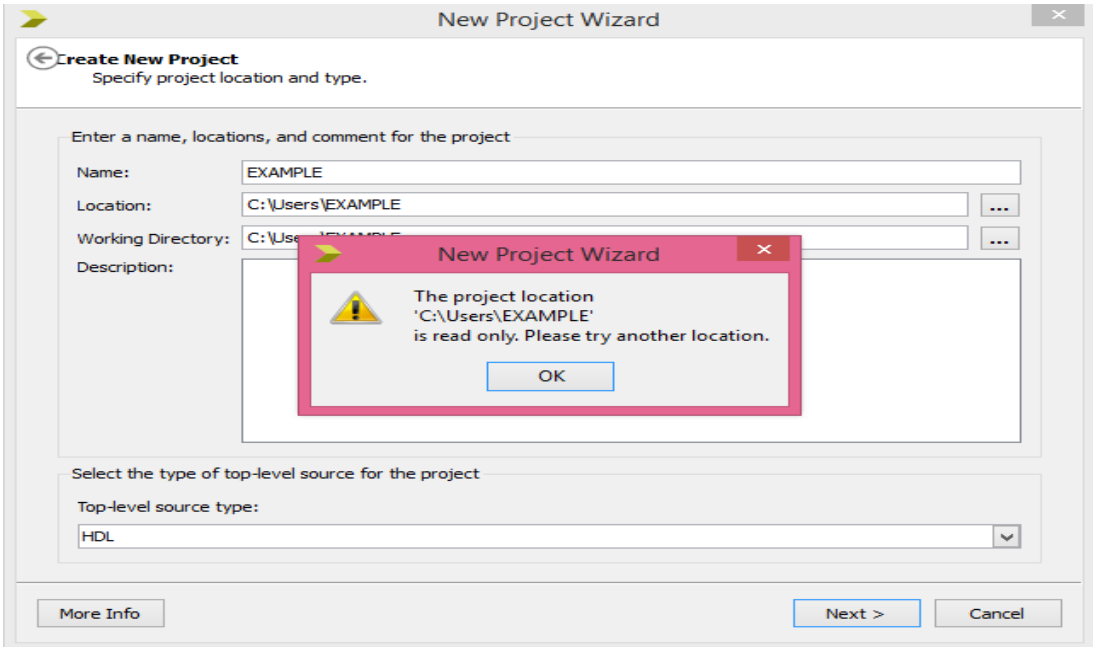


Fig 6.3 CLICK ON NEXT and NEXT

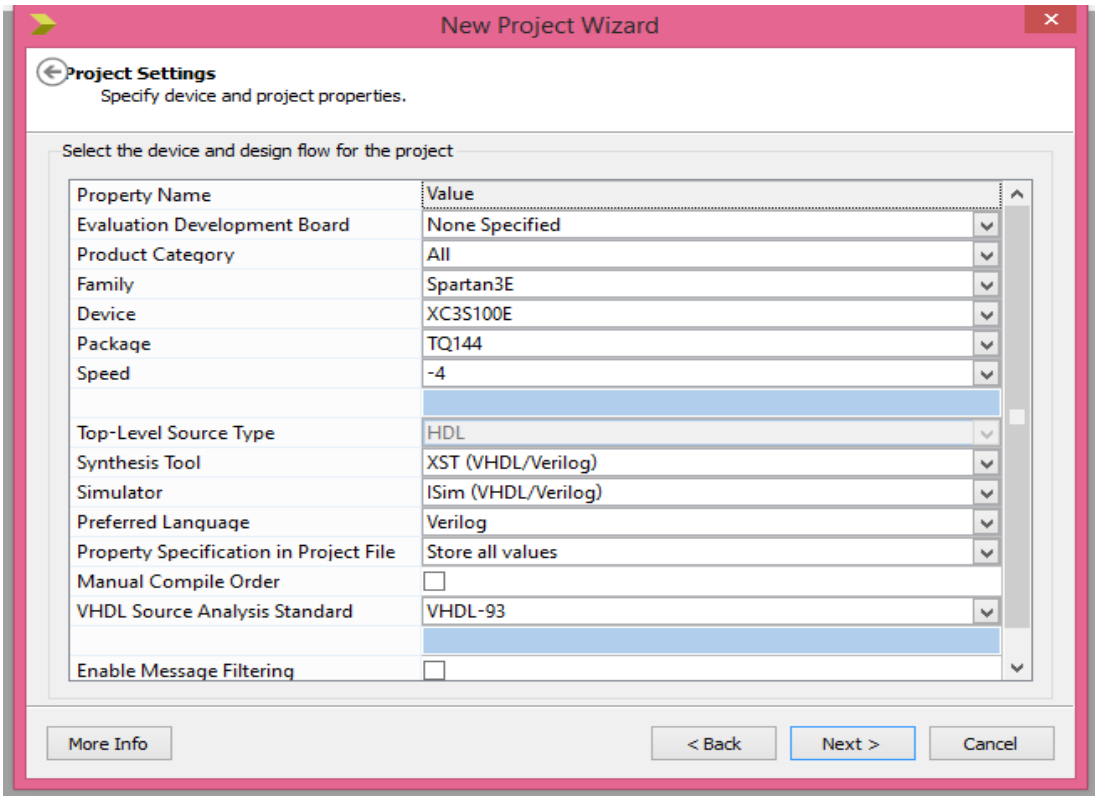


Fig 6.4 CLICK ON NEXT and NEXT

Step 4: CLICK ON FINISH

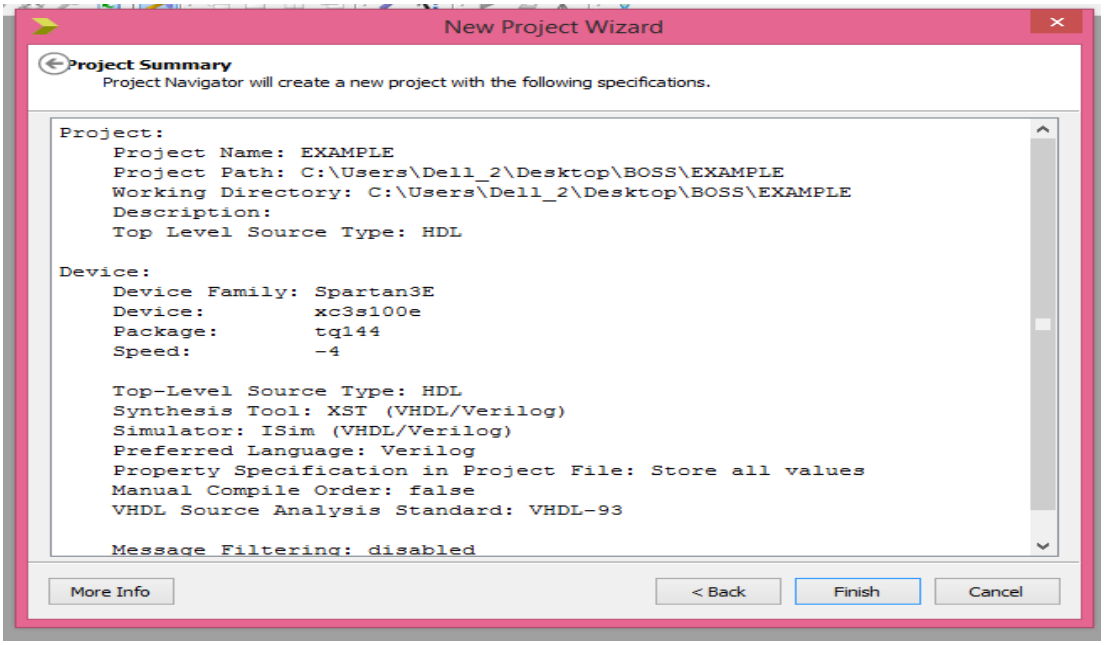


Fig 6.5 Click on finish

Step 5: CLICK ON CHIP (XC…) then MOUSE RIGHT CLICK then CLICK ON ADD SOURCE

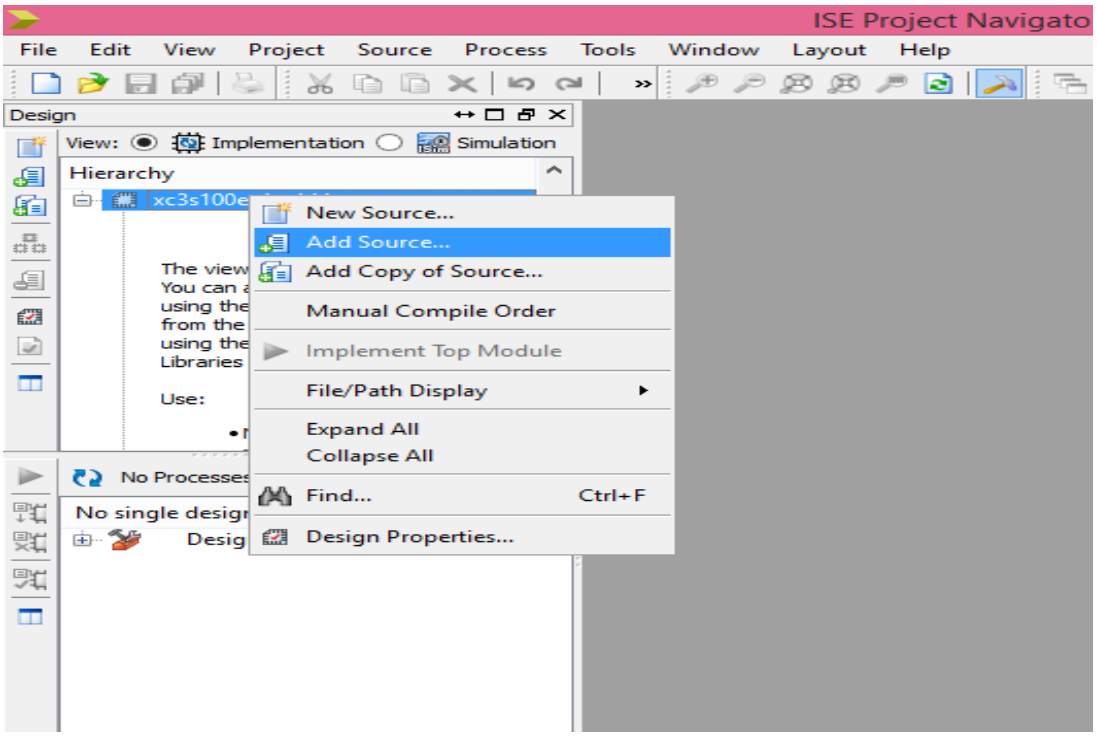


Fig 6.6 CLICK ON CHIP (XC…) then MOUSE RIGHT CLICK then CLICK ON ADD SOURCE

Step 6: SELECT THE CODE LOCATION GIVEN BY DEVELOPER AND ADD CODE

(Note ALL FILES) AND CLICK OPEN

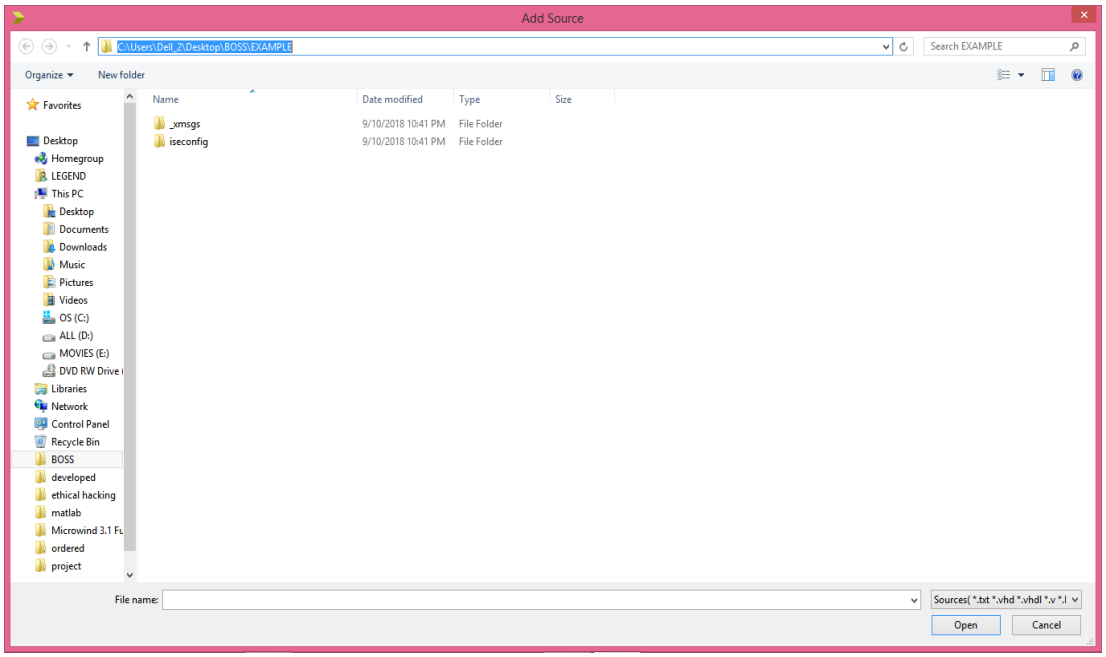


Fig 6.7 Select the code location given by developer and add code

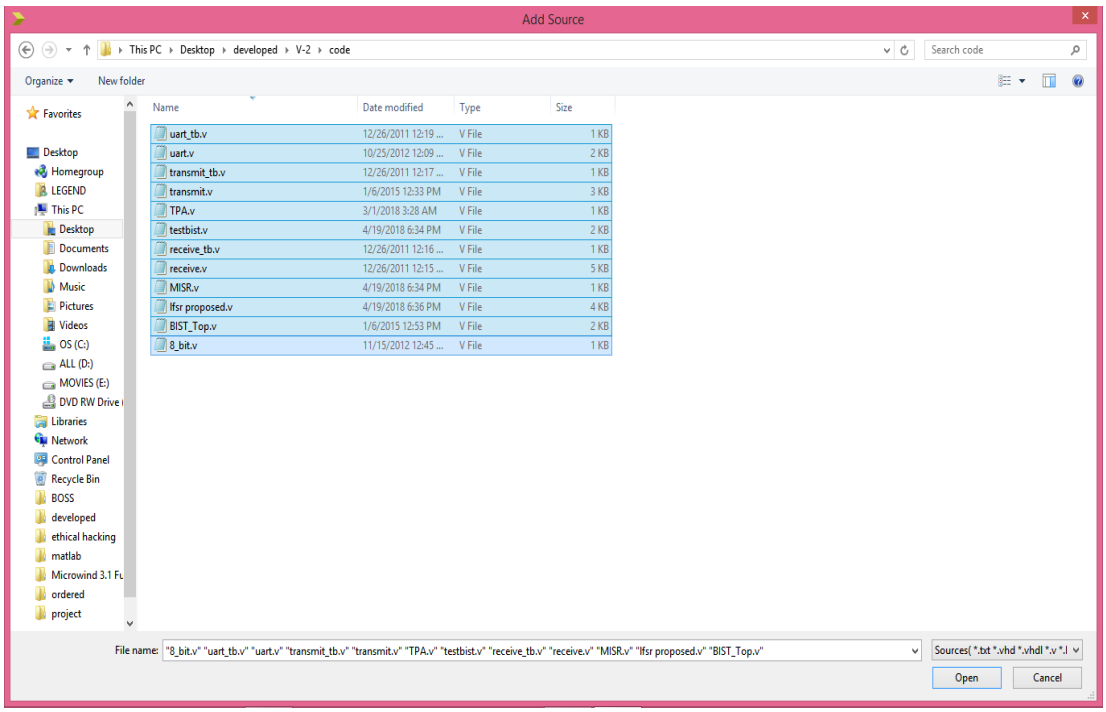


Fig 6.8 Select the code location given by developer and add code

Step 7: SELECT THE SIMULATION and select files to RUN

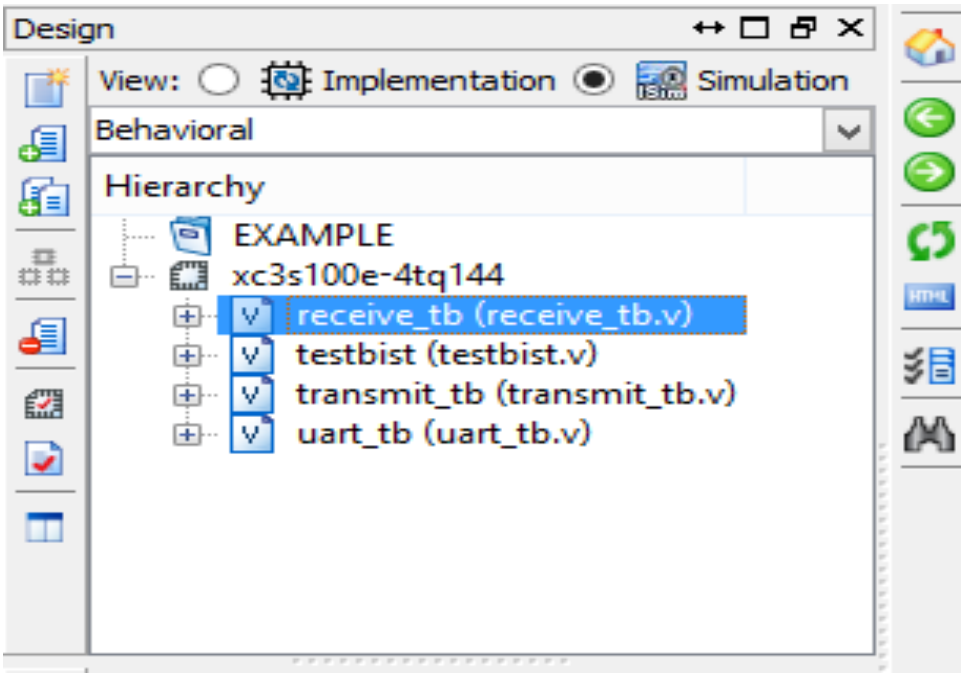


Fig 6.9 SELECT THE SIMULATION and select files to RUN

Step 8: SELECT ISIM SIMULATOR and SIMULATE BEHAVIORAL MODEL

If no errors isim window will open

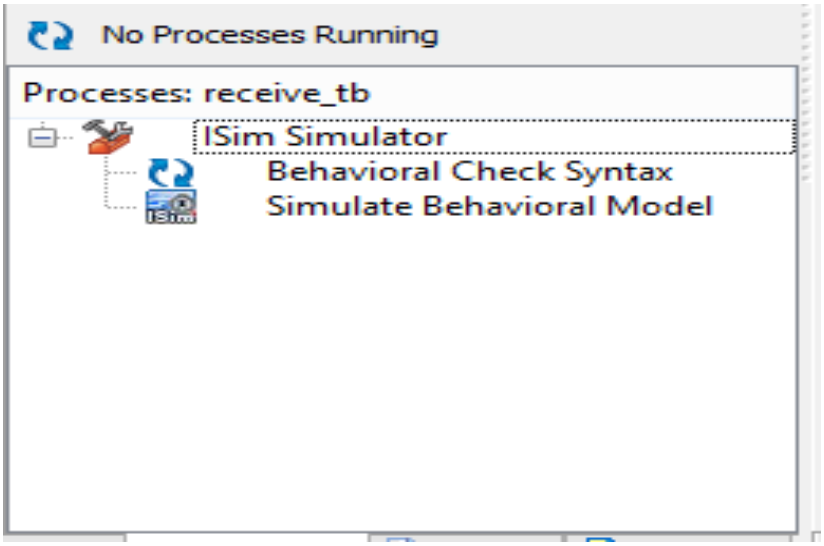


Fig 6.10 SELECT ISIM SIMULATOR and SIMULATE BEHAVIORAL MODEL

Step 9: ISIM WINDOW

select zoom to full view

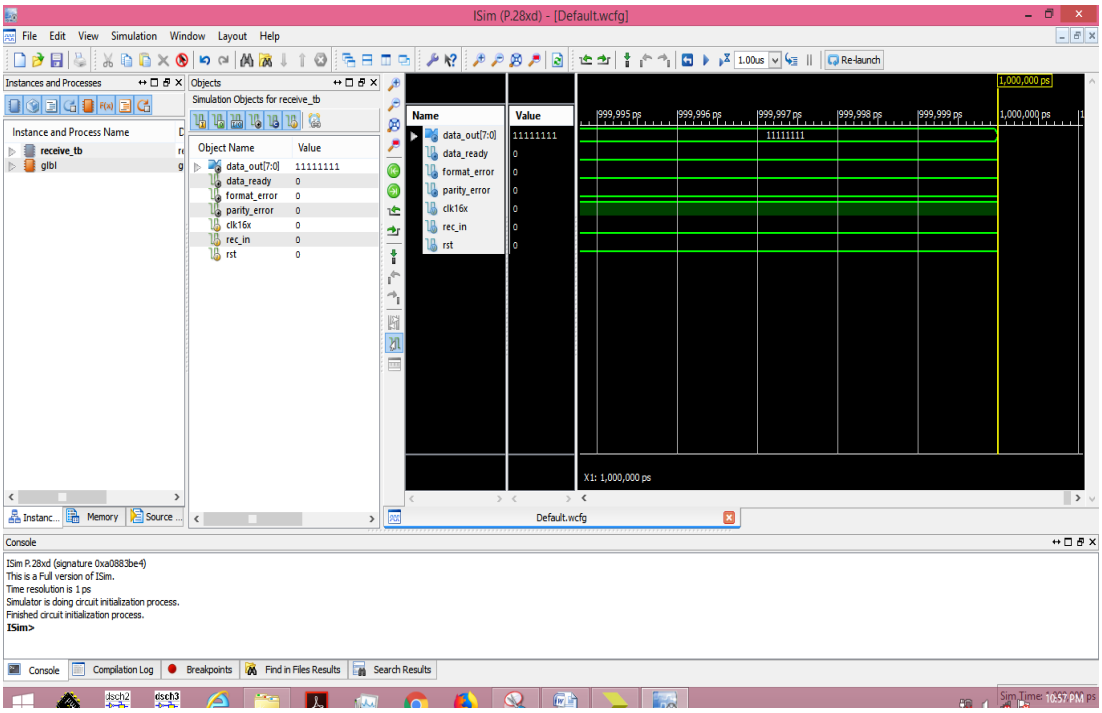


Fig 6.11 Select zoom to full view

CHAPTER 7

SIMULATION RESULTS

7.1 RESULTS

This section gives the detailed analysis of proposed LFSR based ER-TCAM. The model is developed and implemented using Xilinx-ISE 14.2 software with Verilog programming language. Further, the performance of proposed method is compared with state of art models.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	32	35200	0%
Number of Slice LUTs	128	17600	0%
Number of fully used LUT-FF pairs	16	144	11%
Number of bonded IOBs	89	100	89%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig 7.1 Design summary.

Fig 7.1 shows the design (area) summary of proposed method. Here, the proposed method utilizes the low area in terms of slice look-up-tables (LUTs)i.e., 128 out of available 17600. Further, the proposed method utilizes the slice registers as 32, out of available 35200. Further, the proposed method utilizes fully used look-up-table-flip-flop (LUT-FF) as 16, out of available 144.

7.1.1TIME SUMMARY

```
Data Path: data<13> to D1/dec_out_13
                              Gate     Net
  Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O             9    0.000    0.316  data_13_IBUF (data_13_IBUF)
   LD:D                     -0.035           D1/dec_out_13
  ----------------------------------------
  Total                      0.316ns (0.000ns logic, 0.316ns route)
                                     (0.0% logic, 100.0% route)
```

Fig 7.2 Time summary

Fig 7.2 shows the time summary of proposed method. Here, the proposed method consumed total 0.316ns of time delay, which is entirely route delay.

7.1.2 SIMULATION OUTCOME

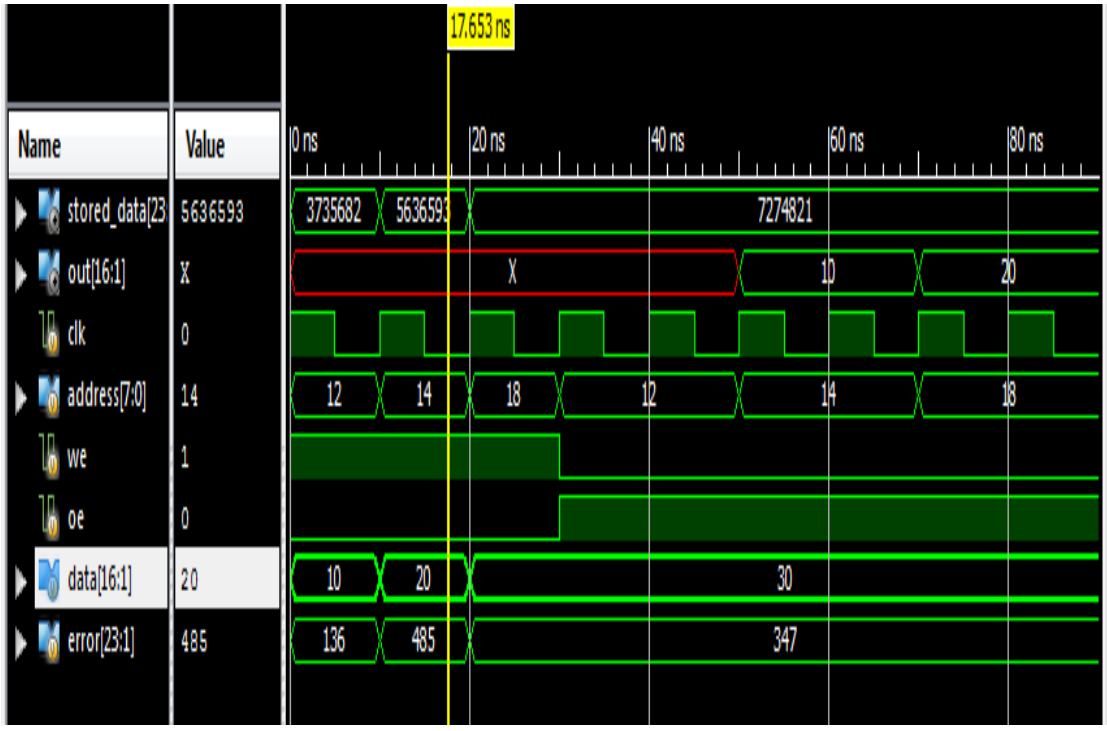


Fig 7.3 Simulation outcome.

Figure 7.3 presents the simulation outcome of proposed system. Here, clock (clk), address, write_enable (we), output_enable(oe), data, and error are the input data pins. Further, out and stored_data are the output pins. Here, 16-bit data is stored into

TCAM (example 10), and during the storage error is occurred (example 136). So, the error stored value in TCAM becomes 3735682. Finally, error detection and correction operations are performed, which resulted in error free output as 10 in out signal.

7.1.3 POWER SUMMARY

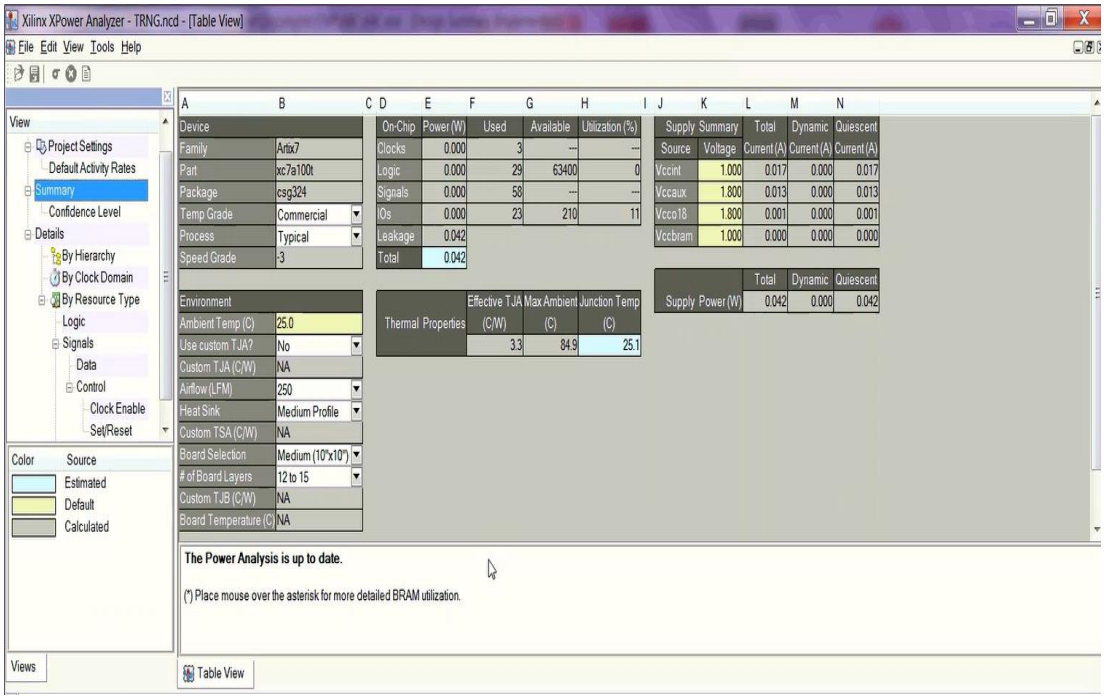


Fig 7.4 Power summary.

Fig 7.4 shows the power consumption report of proposed ER-TCAM. Here, the proposed ER-TCAM consumed power as 0.042watts. Table 1 compares the performance evaluation of various TCAM controllers. Here, the proposed ER-TCAM resulted in superior (reduced) performance in terms of LUTs, slice registers, LUT-FFs, time-delay, and power consumption as compared to conventional approaches such as DyTAN [22], MTCAM [23], and CN-TCAM [24]. Further, the graphical representation of performance comparison is presented in Fig 7.5.

7.1.4 PERFORMANCE EVALUATION

Metric	DyTAN [22]	MTCAM [23]	CN-TCAM [24]	Proposed ER-TCAM
Slice Registers	125	78	46	32
LUTs	462	362	284	128
LUT-FFs	45	32	29	16
Time delay (ns)	0.927	0.837	0.735	0.316
Power consumption (w)	0.826	0.734	0.386	0.042

Table 7.1 Performance evaluation.

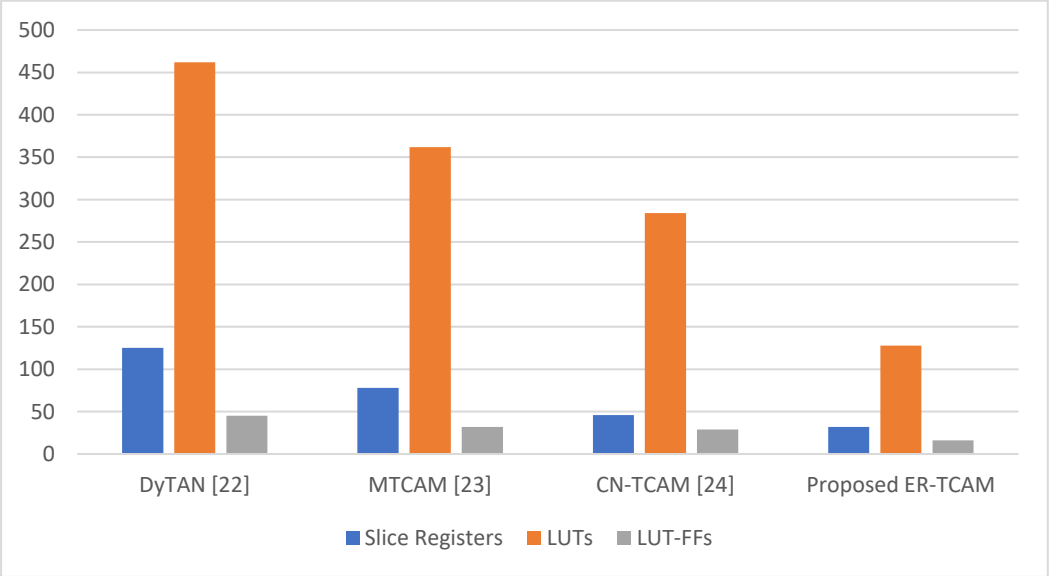


Fig 7.5 Graphical representation of performance evaluation.

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

CONCLUSION

The implementation of ER-TCAM for quick data storage with fast read-write operations is the main topic of this paper. For the purpose of creating random pattern sequences with address synchronization features, LFSR cells were introduced. The ideal data storage with strong self-error detection, correction properties was offered by LFSR-based ER-TCAM. The simulations showed that the proposed method outperformed existing approaches in terms of area, latency, and power. Further, this work can be extended with parallel memory allocation systems using LFSR based ER-TCAM modules for improved performance.

FUTURE SCOPE

The proposed low-cost dual-clock FIFO combines mesochronous clock synchronization with buffering in a scalable way. This is possible despite the fact that the sender and the receiver in a mesochronous clock interface may or may not be in close physical proximity to one another. On the receiving end of a mesochronous interface, data may be securely exchanged without it being necessary to explicitly synchronize the transfer. Only the single-bit push/pop flow-control signals are involved in the synchronization process. This implicit synchronization of data helps save a significant amount of space and power, particularly in the case of multicycle networks, and it does so without adding extra delay or lowering throughput.

CHAPTER 9

REFERENCES

[1]. Ni, Kai, et al. "Ferroelectric ternary content-addressable memory for one-shot learning." *Nature Electronics* 2.11 (2019): 521-529.

[2]. Yang, Rui, et al. "Ternary content-addressable memory with MoS2 transistors for massively parallel data search." *Nature Electronics* 2.3 (2019): 108-114.

[3]. Xiong, Xiong, et al. "Nonvolatile Logic and Ternary Content-Addressable Memory Based on Complementary Black Phosphorus and Rhenium Disulfide Transistors." *Advanced Materials* (2021): 2106321.

[4]. Wang, Chengzhi, et al. "A novel MTJ-based non-volatile ternary content-addressable memory for high-speed, low-power, and high-reliable search operation." *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.4 (2018): 1454-1464.

[5]. Wang, Xuehong, et al. "A 4T2R RRAM Bit Cell for Highly Parallel Ternary Content Addressable Memory." *IEEE Transactions on Electron Devices* 68.10 (2021): 4933-4937.

[6]. Choi, Woong, Kyeongho Lee, and Jongsun Park. "Low cost ternary content addressable memory using adaptive matchline discharging scheme." *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018.

[7]. Ly, D. R., Giraud, B., Noël, J. P., Grossi, A., Castellani, N., Sassine, G., ... & Vianello, E. (2018, December). In-depth characterization of resistive memory-based ternary content addressable memories. In *2018 IEEE International Electron Devices Meeting (IEDM)* (pp. 20-3). IEEE.

[8]. Lee, J. S., Yoon, J., & Choi, W. Y. (2021). In-Memory Nearest Neighbor Search With Nanoelectromechanical Ternary Content-Addressable Memory. *IEEE Electron Device Letters*, *43*(1), 154-157.

[9]. Gnawali, Krishna Prasad, Seyed Nima Mozaffari, and Spyros Tragoudas. "Low power spintronic ternary content addressable memory." *IEEE Transactions on Nanotechnology* 17.6 (2018): 1206-1216.

[10]. Ly, D. R. B., et al. "Novel 1T2R1T RRAM-based ternary content addressable memory for large scale pattern recognition." *2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2019.

[11]. He, Nian, et al. "Inverter and Ternary Content-Addressable Memory Based on Carbon Nanotube Transistors Using Chemical Doping Strategy." *Advanced Electronic Materials* (2022): 2200424.

[12]. Karthik, S., et al. "Design and Implementation of a Low Power Ternary Content Addressable Memory (TCAM)." *2020 International SoC Design Conference (ISOCC)*. IEEE, 2020.

[13]. Narla, Siri, et al. "Modeling and Design for Magnetoelectric Ternary Content Addressable Memory (TCAM)." *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits* (2022).

[14]. Mahendra, Telajala Venkata, et al. "Energy-efficient precharge-free ternary content addressable memory (TCAM) for high search rate applications." *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.7 (2020): 2345-2357.

[15]. Lee, Jae Seong, and Woo Young Choi. "Nanoelectromechanical-switch-based ternary content-addressable memory (NEMTCAM)." *IEEE Transactions on Electron Devices* 68.10 (2021): 4903-4909.

[16]. Yin, Xunzhao, et al. "Ferroelectric Ternary Content Addressable Memories for Energy Efficient Associative Search." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2022).

[17]. Irfan, Muhammad, et al. "Comp-tcam: an adaptable composite ternary content-addressable memory on fpgas." *IEEE Embedded Systems Letters* 14.2 (2021): 63-66.

[18]. Yang, Ling, et al. "In-Memory Search with Phase Change Device-based Ternary Content Addressable Memory." *IEEE Electron Device Letters* (2022).

[19]. Chang, Yen-Jen, et al. "Low-power ternary content-addressable memory design based on a voltage self-controlled fin field-effect transistor segment." *Computers & Electrical Engineering* 81 (2020): 106528.

[20]. Irfan, Muhammad, et al. "RPE-TCAM: Reconfigurable power-efficient ternary content-addressable memory on FPGAs." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 28.8 (2020): 1925-1929.

[21]. Bahloul, Mohamed A., et al. "Variability analysis of resistive ternary content addressable memories." *International Journal of Circuit Theory and Applications* 49.2 (2021): 453-475.

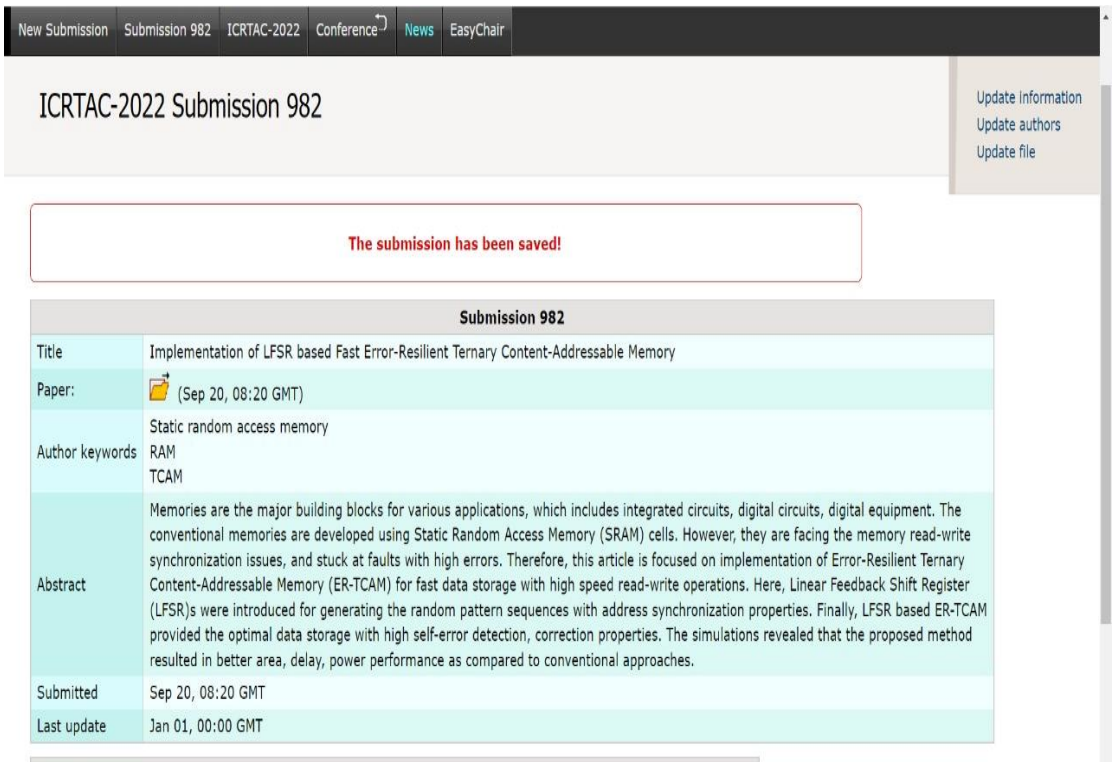
[22]. Zhong, Hongtao, et al. "DyTAN: Dynamic Ternary Content Addressable Memory Using Nanoelectromechanical Relays." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 29.11 (2021): 1981-1993.

[23]. Gnawali, Krishna, and Spyros Tragoudas. "High-speed memristive ternary content addressable memory." *IEEE Transactions on Emerging Topics in Computing* (2021).

[24]. Wang, Xianggao, et al. "A Highly Compact Nonvolatile Ternary Content Addressable Memory (TCAM) With Ultralow Power and 200-ps Search Operation." *IEEE Transactions on Electron Devices* 69.8 (2022): 4259-4264.

[25]. Durai, Jothi, Sivakumar Rajagopal, and Geetha Ganesan. "Design and Analysis of Power-Efficient Quasi-Adiabatic Ternary Content Addressable Memory (QATCAM)." *IET Circuits, Devices & Systems* 14.7 (2020): 923-928.

APPENDIX



New Submission | Submission 982 | ICRTAC-2022 | Conference | News | EasyChair

ICRTAC-2022 Submission 982

Update information
Update authors
Update file

The submission has been saved!

Submission 982	
Title	Implementation of LFSR based Fast Error-Resilient Ternary Content-Addressable Memory
Paper:	(Sep 20, 08:20 GMT)
Author keywords	Static random access memory RAM TCAM
Abstract	Memories are the major building blocks for various applications, which includes integrated circuits, digital circuits, digital equipment. The conventional memories are developed using Static Random Access Memory (SRAM) cells. However, they are facing the memory read-write synchronization issues, and stuck at faults with high errors. Therefore, this article is focused on implementation of Error-Resilient Ternary Content-Addressable Memory (ER-TCAM) for fast data storage with high speed read-write operations. Here, Linear Feedback Shift Register (LFSR)s were introduced for generating the random pattern sequences with address synchronization properties. Finally, LFSR based ER-TCAM provided the optimal data storage with high self-error detection, correction properties. The simulations revealed that the proposed method resulted in better area, delay, power performance as compared to conventional approaches.
Submitted	Sep 20, 08:20 GMT
Last update	Jan 01, 00:00 GMT